HP Vectra 500 Series PC

Models: 520 5/xx

525 5/xx

Hardware and BIOS Technical Reference Manual

September 1996

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Preface

This manual is a technical reference and BIOS document for engineers and technicians providing system level support for HP Vectra 500 Series PCs for models 520 5/xx and 525 5/xx.

It is assumed that the reader possesses a detailed understanding of AT-compatible microprocessor functions and digital addressing techniques.

Technical information that is readily available from other sources, such as manufacturers' proprietary publications, has not been reproduced.

This manual contains summary BIOS information only. For detailed information, it is recommended to read the reference work cited in the next section. For additional reference material, refer to the bibliography.

Ordering the Phoenix BIOS Manual

System BIOS for IBM PCs, Compatibles, and EISA Computers (ISBN 0-201-57760-7) by Phoenix Technologies is available in many bookstores. It can also be ordered directly from the publisher as follows:

In the U.S.A.

Call Addison-Wesley in Massachusetts at +1-617-944-3700, and be prepared to give a credit card number and expiry date.

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Conventions

The following conventions are used throughout this manual to identify specific elements:

- ❒ Hexadecimal numbers are identified by a lower case h.
  For example, 0FFFFFFFh or 32F5h
- ❒ Binary numbers and bit patterns are identified by a lower case b.
  For example, 1101b or 10011011b

Bibliography

- ❒ *System BIOS for IBM PCs, Compatibles, and EISA Computers* (ISBN 0-201-57760-7) by Phoenix Technologies. Addison-Wesley (publisher).

The following Hewlett-Packard publications may also assist the reader of this manual:

- ❒ HP Vectra 500 Series *Service Handbook - 3rd editio*n.
  HP Part Number: 5964-8385-EN.
- ❒ HP Vectra 500 Series Familiarization Guide.
  HP Part Number: 5964-8384-EN.

- ❒ Online Acrobat Reader documents for either the desktop or minitower packages. These books are:

  Upgrade Guide - explaining how to upgrade and install memory, mass storage devices, expansion cards, and upgrade (overdrive) processors.
  Advanced Setup Guide - information about system configurations and characteristics, using the HP Setup program and communications options.
  Note: These online documents are customized for a particular platform, depending on the system board, desktop or minitower package, and communications options.

The following Intel publication provides more detailed information:

- ❒ *Pentium Processor* (241595-002)

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1

HP Vectra 500 Series

This chapter provides a description of the HP Vectra 500 Series desktop (Models 520 5/xx) and minitower (Models 525 5/xx) computers with detailed system specifications. The HP Vectra 500 Series computers are Pentium processor-based, constructed around the Peripheral Component Interconnect (PCI) bus and Industry Standard Architecture (ISA) bus.

Introduction

Three group types have been defined to help identify the various system configurations available on the HP 500 Series desktop and minitower packages. Within each group, a product number and the appropriate HP Vectra 500 Series model have been associated with the HP Service Part Number.

The HP Service Part Numbers are:

- D4051-63001
- D3657-63001
- D3661-63001

An HP Service Part Number group contains details of a specific system configuration. For example, if there is a need to perform a check on a certain product number, first determine which group type it belongs to, then refer to System Features, on page 17, for a list of main features.

System Overview

D4051-63001 Models

The HP Service Part Number D4051-63001 group contains HP Vectra 500 Series models that have the following features: Unified Memory Architecture (UMA), main memory upgradable to 192 MB, and the SiS (Silicon Integrated System) 6205 video graphic controller.

D4051-63001- Desktop Models

The following table shows the models and their associated product numbers.

Model	Product Number			
520 5/133	D4402A	D4403A	D4404A	D4434A
520 CD[1] 5/133	D4413A	D4414A	D4437A	D4460A
520 MCx[2] 5/120	D4420A	D4428A		
520 MCx[2] 5/133		D4440A	D4442A	
520 MCx[2] 5/166	D4443A			

1 = Includes CD-ROM
2 = Includes CD-ROM and Modem/Audio

D4051-63001 - Minitower Models

The following table shows the models and their associated product numbers.

Model	Product Number				
525 5/133	D4454A				
525 CD[1] 5/166	D4422A	D4423A	D4424A	D4425A	
525 MCx[2] 5/133	D4416A	D4418A	D4419A		
525 MCx[2] 5/166	D4426A	D4427A	D4439A	D4441A	

1 = Includes CD-ROM
2 = Includes CD-ROM and Modem/Audio

D3657-63001 Models

The HP Service Part Number D3657-63001 group contains HP Vectra 500 Series models that have the following features: separate main memory and video memory, and an integrated 32/64 Ultra VGA video graphic controller.

D3657-63001 - Desktop Models

The following table shows the models and their associated product numbers.

Model	Product Number	
520 MCx[2] 5/133	D4479A	
520 MCx[2] 5/166	D4480A	

1 = Includes CD-ROM
2 = Includes CD-ROM and Modem/Audio

D3657-63001 - Minitower Models

The following table shows the models and their associated product numbers.

Model	Product Number		
525 5/166	D4483A		
525 5/200	D4474A		
525 CD[1] 5/133	D4475A		
525 CD[1] 5/166	D4476A		
525 CD[1] 5/200	D4470A	D4472A	
525 MCx[2] 5/133	D4477A		
525 MCx[2] 5/166	D4478A		
525 MCx[2] 5/200	D4473A	D4481A	D4482A

1 = Includes CD-ROM
2 = Includes CD-ROM and Modem/Audio

D3661-63001 Model

The HP Service Part Number D3661-63001 group contains one HP Vectra 500 Series model that has the following features: separate main memory and a Matrox MGA millennium video card.

D3661-63001 - Minitower Model

The following table shows the model and its associated product number.

Model	Product Number	
525 MCx^2 5/200	D4471A	
1 = Includes CD-ROM 2 = Includes CD-ROM and Modem/Audio		

System Features

The following table shows the main features available on the various HP Vectra 500 Series PC models. The table definitions are:

Shading	Description
	Indicates that the feature is only valid for this type of system.
	Indicates that the feature is only valid for this type of system.

Features	HP Service Part Number: D4051-63001	HP Service Part Number: D3657-63001 and D3661-63001	
System Board	Unified Memory Architecture (UMA)	Separate Main Memory and Video Memory	
Main Memory	12 or 16 MB. Maximum 192 MB	8, 12 ,16 or 32 MB. Maximum 128MB	
Video Controller	SiS 6205 Graphic	Trio 64 PnP on PCI Bus	Matrox MGA Millennium card
Video Memory	1 MB upgrade to 2 MB	1 MB upgrade to 2 MB Installing two 512 KB modules	2 MB standard, upgradable to 4 MB or 8 MB.
Pentium Processor	120MHz,133MHz,166MHz	133MHz, 166MHz, 180MHz, 200MHz	

Features	HP Service Part Number: D4051-63001	HP Service Part Number: D3657-63001 and D3661-63001
Level-two cache memory (optional)	256 KB synchronous cache are standard on the following models: U.S./Canada D4403, D4422A, D4428A, D4437A, D4439A, D4442A, D4470A, D4475A, D4476A, D4477A, D4478A, D4471A, D4481A Europe D4416A, D4441A, D4443A, D4472A, D4473A Latin America D4425A, D4427A Brazil D4480A China, India, Korea D4426A, D4482A Asia/Pacific Partner D4434A, D4454A, D4474A, D4483A	

Comparison of HP Vectra 500 Series Desktop and Minitower Models

The HP Vectra 500 Series PCs come in two packages, a desktop box and a minitower box. The following table shows the differences between the two packages.

Component	Desktop	Minitower
IDE Controller Primary channel connectors	Two connectors for hard disk drives	Two connectors for hard disk drives
IDE Controller Secondary channel connectors	One connector is for a CD-ROM	Two connectors for a supplementary hard disk drive and CD-ROM
Floppy disk controller connectors	Two connectors : - One for a 3.5-inch floppy disk drive - One for either a tape drive or a 5.25-inch disk drive	Two connectors for 3.5-inch floppy disk drive One connector for 5.25-inch floppy disk drive or a tape drive Maximum two devices connected simultaneously
Expansion card slots (on backplane)	Two 16-bit ISA (full-length 30 cm / 12-inches) One Combination slot (32-bit PCI or one 16-bit ISA) One 32-bit PCI (full-length)	Two 16-bit ISA (full-length 30 cm / 12-inches) One 16-bit ISA (short-length 15 cm / 6-inches) One Combination slot (32-bit PCI or one 16-bit ISA) Two 32-bit PCI (full-length)
Internal device shelves	One for hard disk drive	Two for hard disk drives
Front-access device shelves	One 3.5-inch One 5.25-inch One 5.25-inch, 1-inch high (or an internal drive)	One 3.5-inch Three 5.25-inch

Principal Features

This section includes the principal features of the system board that are available on both the desktop and minitower packages:

- An Enhanced IDE controller with two channels on the PCI bus.
- Rear panel connectors:
  - ❒ 1 mouse socket
  - ❒ 1 keyboard socket
  - ❒ 1 display connector
  - ❒ 1 parallel connector
  - ❒ 2 serial ports
- a system ROM (using flash ROM technology) that can be easily updated with the latest firmware, using the *Phlash.exe* program supplied with the firmware upgrade. The system ROM contains:
  - ❒ the BIOS (system BIOS, video BIOS and low option ROM)
  - ❒ menu-driven SETUP with context-sensitive help (in U.S. English only)
- a keyboard/mouse controller and interface.

Physical and Environmental Specifications

The following tables show the physical and environmental specifications of the minitower and desktop computers. All the characteristics valid for both computers are grouped together at the end of the table.

Computer Type	Characteristic	Description
Minitower	Weight (excluding keyboard and display)	13 kilograms (28.7 pounds)
	Dimensions	44 cm (Depth) by 19.2 cm (Width) by 43.8 cm (Height) (17.3 inches by 7.6 inches by 17.2 inches)
	Footprint	0.084 m^2 (0.9 sq ft)
	Acoustic noise emission	$\leq$ 40 dBA (as defined by DIN 45635 T.19 and ISO 7779)
	Power supply	• Input voltage: 100-127 VAC and 200-240 VAC over 50/60 Hz manual switching between 115 & 230 V • Power consumption: 30 W to 40 W (typical), 220 W (maximum) • Power availability: 160 W continuous, 200 W peak
Desktop	Weight (excluding keyboard and display)	9 kilograms (20 pounds)
	Dimensions	39 cm (Depth) by 42 cm (Width) by 12.5 cm (Height) (15.3 inches by 16.5 inches by 4.9 inches)
	Footprint	0.17 m^2 (1.8 sq ft)
	Acoustic noise emission	Lw $\leq$ 40 dBA, Lp $\leq$ 34 dBA
	Power supply	• Input voltage: 100-127 VAC +200-240 VAC ac auto-ranging. Input frequency: 50 / 60 Hz • Power consumption: 30 W to 40 W (typical), 150 W (maximum) • Power availability: 100 W continuous

Computer Type	Characteristic	Description
These characteristics are valid for both the minitower and desktop computers.	Operating temperature	+5°C to +40°C (+40°F to +104°F)
	Recommended operating temperature	+15°C to +30°C (+59°F to +104°F)
	Storage temperature	-40°C to +70°C (-40°F to +158°F)
	Over temperature shutdown	+50°C (+122°F)
	Operating humidity	15% to 80% (relative)
	Storage humidity	8% to 80% (relative)
	Operating altitude	3100 m (10000 ft) max
	Storage altitude	12200 m (40000 ft) max
	Maximum thermal dissipation	91 kcal per hour (360 BTU per hour)
Keyboard	Flat	464 mm (Width) by 178 mm (Depth) by 33 mm (Height) (18.3 inches by 7 inches by 1.3 inches)
	Standing	464 mm (Width) by 178 mm (Depth) by 51 mm (Height) (18.3 inches by 7 inches by 2 inches)

NOTE

Operating temperature and humidity ranges may vary depending upon the mass storage devices installed. High humidity levels can cause improper operation of disk drives. Low humidity ranges can aggravate static electricity problems and cause excessive wear of the disk surface.

Power Consumption

NOTE

The figures given below are valid for both the minitower and desktop computers with a standard configuration—no expansion cards and no CD-ROM drive. For other configurations, the power consumption values will be higher.

Full Power Mode	< 44 W
Standby Mode	< 29 W
Suspend Mode	< 24 W
Off	< 5 W[1]

1. The power supply in the computer continues to supply power to the CMOS memory, even when turned off.

NOTE

When the PC is turned off with the power button on the front panel, the power consumption falls below 5 watts, but is not zero. The special on/off method used by this PC considerably extends the lifetime of the power supply. To reach zero power consumption in "off" mode, either unplug the PC from the power outlet or use a power block with a switch.

Typical Power Consumption/Availability for ISA Expansion Card Slots

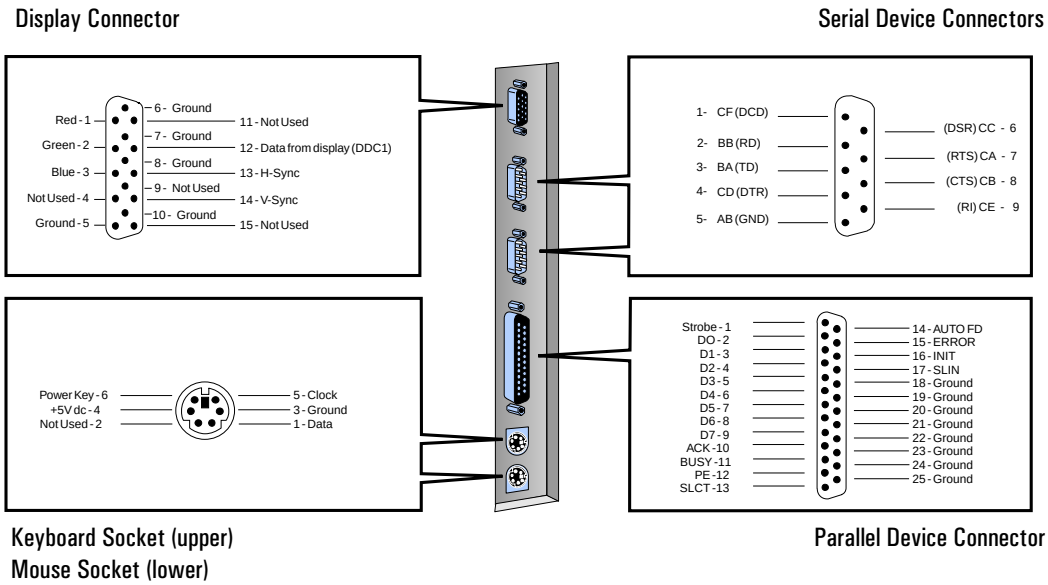
+ 5 V	4.5A limit per slot (limited by system board)
+ 12 V	1.5A limit per slot (limited by system board)
- 5 V	0.1A total power limit (limited by power supply)
- 12 V	0.3A total power limit (limited by power supply)

Typical Power Consumption/Availability for PCI Expansion Card Slots

+ 5 V	4.5A maximum per slot
+ 12 V	0.5A maximum per slot
- 12 V	0.1A maximum per slot

Rear Panel Connectors

The external connectors on the rear panel of the computer are used to connect the mouse, keyboard and display. The 25-pin parallel port can be used for connecting a parallel printer, while the two 9-pin buffered serial ports are for serial printers. The following diagram shows the rear panel connectors for the minitower and desktop computers.



CD-ROM Drive Specifications

WARNING **To avoid electrical shock and harm to your eyes by laser light, do not open the CD-ROM drive enclosure. Do not attempt to make any adjustment to the CD-ROM drive. Refer servicing to qualified personnel only. The CD-ROM drive is a Class 1 laser product.**

Data Capacity	•656 MB (Mode 1) •748 MB (Mode 2)
Data Transfer Rate	Depends on the model. The single-speed rate is 150 KB/sec. Therefore, for example, an 8X model has a data transfer rate of 1200 KB/sec.
Buffer Size	•≥ 128 KB
Average Seek Time	•< 200 ms (quadruple-speed and faster models)
Rotational Speed	Depends on the model. The single-speed is 200-530 rpm. Therefore, for example, an 8X model has a rotational speed of 1600-4240 rpm.
Interface	•ATAPI
Laser	•Type: Semiconductor Laser GaAlAs •Wavelength: 785 nm ± 30 nm •Output Power: 3 mW ± 3 mW •Pulse Duration: $T \geq 3 \times 10^{-4}$ sec
Power Requirements	•5 V, 12 V (see the label on the CD-ROM drive).
Supported CD-ROM Disks	•CD-ROM XA (Mode 2 Form 1, Mode 2 Form 2) •CD-Digital Audio •Audio-combined CD-ROM •CD-I disks (readable) •CD-I Ready disks (readable) •CD Bridge disks •Photo CD (single and multisession)

2

System Board - (SiS Chipset) (Part Number: D4051-63001)

This section describes the components and features of the SiS (Silicon Integrated System) chipset-based system board. This system board has the HP Service Part Number: D4051-63001.

Overview

The type of system board described in this section uses shared memory based on UMA (Unified Memory Architecture), meaning that there is no dedicated frame buffer used by the video controller (SiS 6205). Instead, the controller uses a portion of the system memory as a frame buffer.

The following tables show the models that are associated with the HP Service Part Number: D4051-63001. For further detailed information concerning system features and a comparison between the desktop and minitower models, refer to “System Features” on page 17.

Model (Desktops)	Product Number			
520 5/133	D4402A	D4403A	D4404A	D4434A
520 CD[1] 5/133	D4413A	D4414A	D4437A	D4460A
520 MCx[2] 5/120	D4420A	D4428A		
520 MCx[2] 5/133		D4440A	D4442A	
520 MCx[2] 5/166	D4443A			
1 = Includes CD-ROM 2 = Includes CD-ROM and Modem/Audio				

Model (Minitowers)	Product Number				
525 5/133	D4454A				
525 CD[1] 5/166	D4422A	D4423A	D4424A	D4425A	
525 MCx[2] 5/133	D4416A	D4418A	D4419A		
525 MCx[2] 5/166	D4426A	D4427A	D4439A	D4441A	
1 = Includes CD-ROM 2 = Includes CD-ROM and Modem/Audio					

Configuration

- Supported Processor: P54CS.
- Level-2 (L2) 256 KB cache sockets.
- UMA Chipset from SiS consisting of three chips that interface between the three main buses (the Host bus, the PCI bus and the ISA bus):

  SiS 5511: Host/PCI bridge, L2 cache memory controller and memory controller.

  SiS 5512: PCI Local Data Buffer (Data Path).

  SiS 5513: PCI/ISA bridge, plus integrated functions.
- Six SIMM module sockets for Extended Data Out (EDO) Dram main memory.
- Onboard graphic controller:

  SiS 6205 used in UMA mode.
- NS 87308 or NS 87307: Super I/O which includes the following features:

  Keyboard and mouse controller.

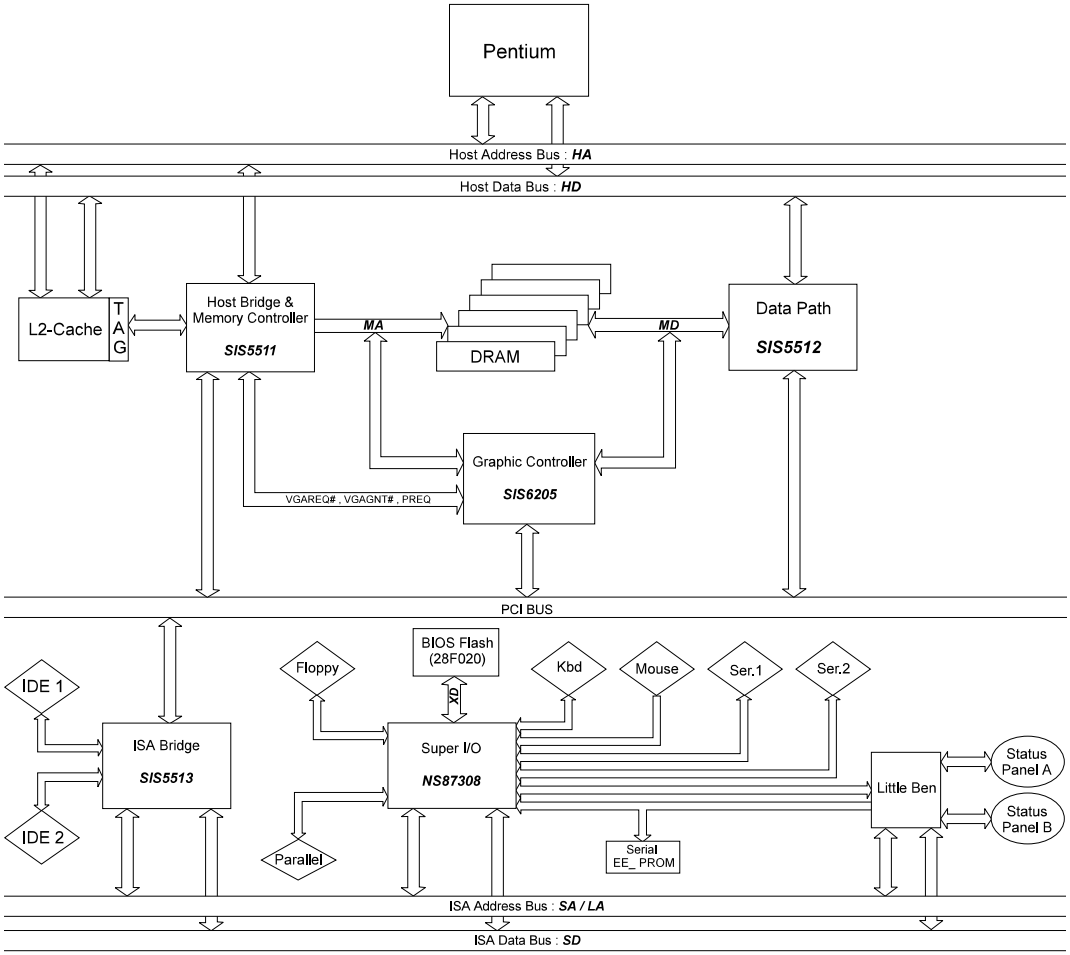
  Floppy drive controller.

  Two serial ports.

  One parallel port.
- Little-Ben chip is an HP designed chip that takes care of security features, power management and some glue logic.
- APM (Advanced Power Management) 1.1 power management compliant.
- 2 Mb Flash Memory (28F020-150) for BIOS.

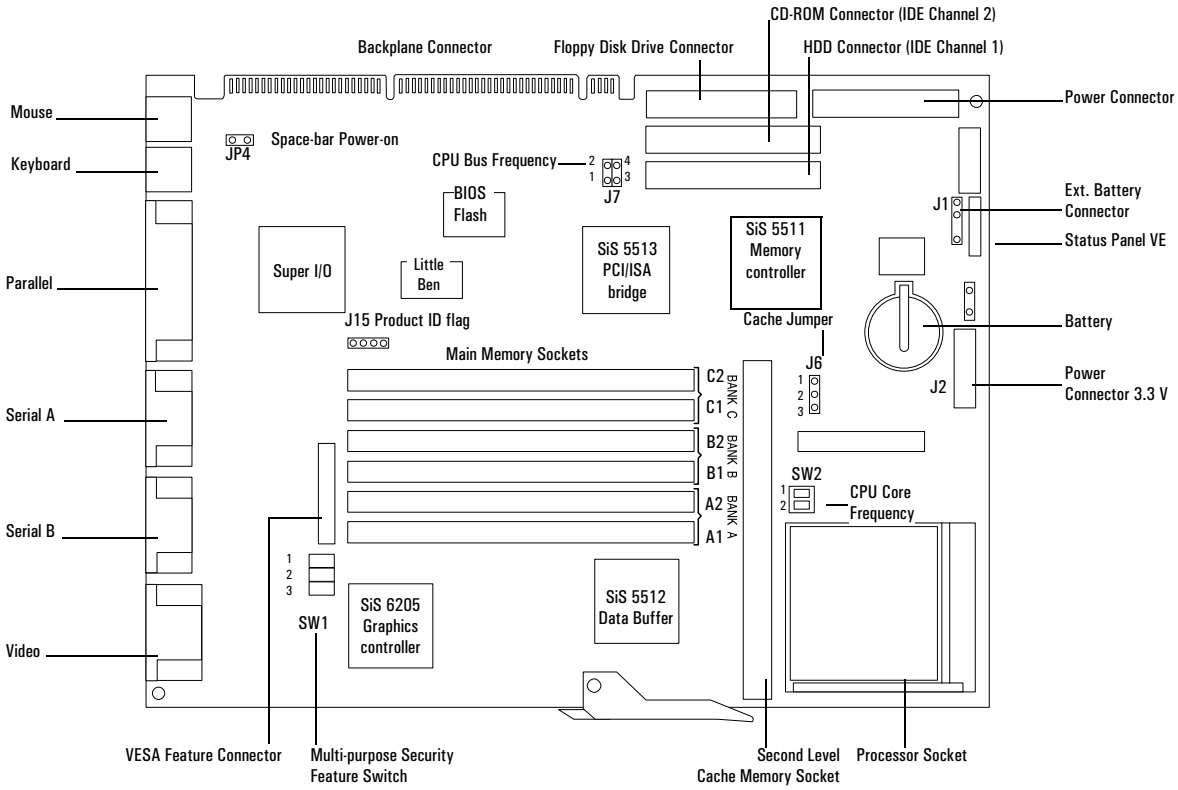
System Board Architecture

The following diagram shows the architecture of the various components and the SiS chipset on the system board.



System Board Physical Layout

The following system board diagram will help you identify where the different components and connections are located on the board. Refer to the section System Board Switches and Jumpers (D4051-63001) on page 38 for switches and jumper settings.

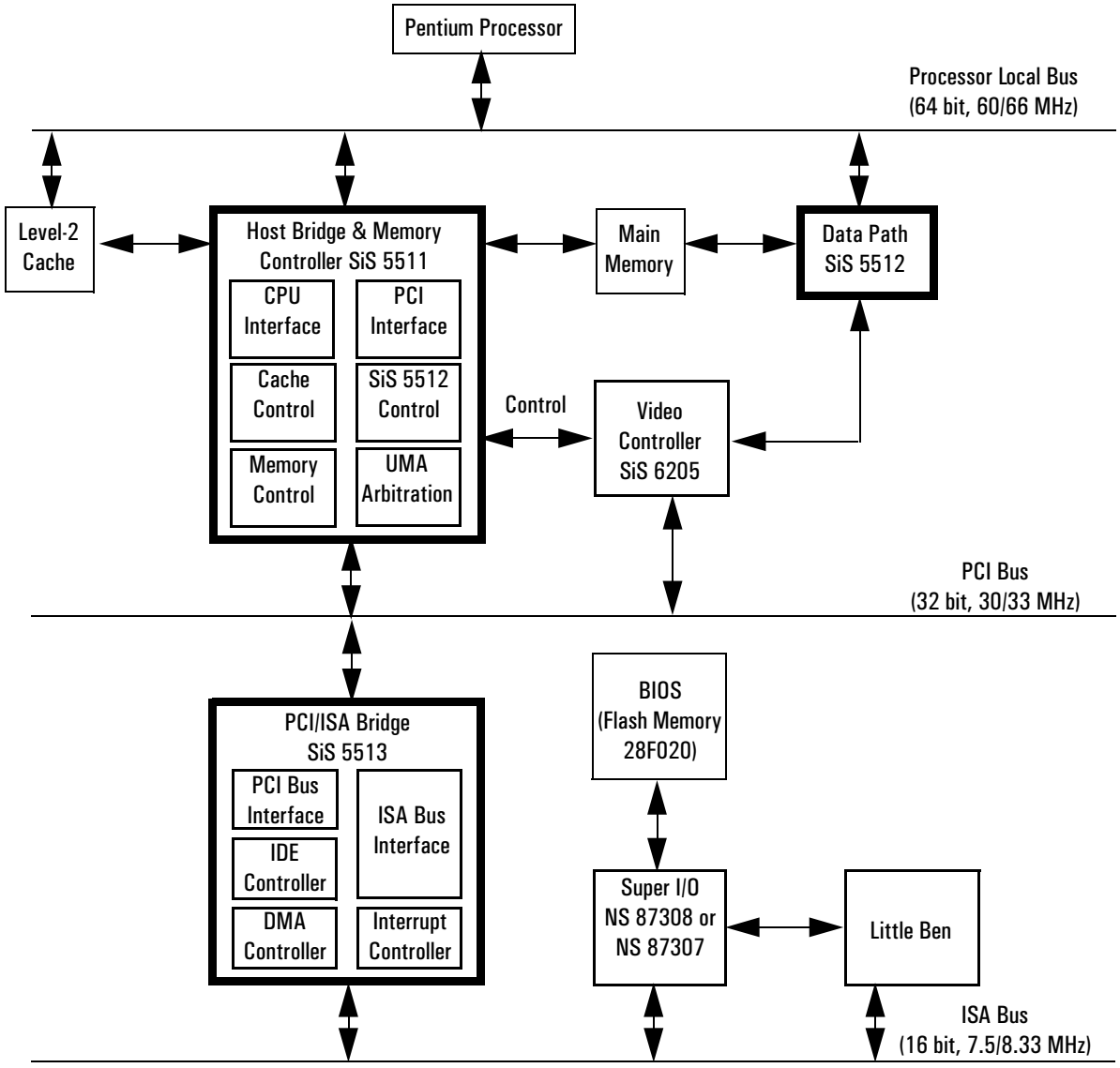


SiS Chipset

The SiS chipset consists of three chips, each encapsulated in a 208-pin plastic quad flat pack (PQFP) package, that interface between the three main buses (the Host bus, the PCI bus and the ISA bus):

- The PCMC chip (SiS 5511) is a combined PL/PCI bridge and cache controller and main memory controller and PCI arbiter.
- The PLDB chip (SiS 5512) provides the PCI local data buffer/path.
- The PSIO chip (SiS 5513) provides the PCI/ISA bridge, responsible for transferring data between the PCI bus and the ISA bus, and also contains the IDE controller.

The block diagram on the following page, gives an overview of the computer's structure. The SiS chipset is described in more detail later on in this chapter.


Pentium Processor
Processor Local Bus
(64 bit, 60/66 MHz)
Level-2
Cache
Host Bridge & Memory
Controller SiS 5511
CPU
Interface
PCI
Interface
Cache
Control
SiS 5512
Control
Memory
Control
UMA
Arbitration
Main
Memory
Data Path
SiS 5512
Control
Video
Controller
SiS 6205
PCI Bus
(32 bit, 30/33 MHz)
PCI/ISA Bridge
SiS 5513
PCI Bus
Interface
IDE
Controller
DMA
Controller
ISA Bus
Interface
Interrupt
Controller
BIOS
(Flash Memory
28F020)
Super I/O
NS 87308 or
NS 87307
Little Ben
ISA Bus
(16 bit, 7.5/8.33 MHz)

Host/PCI Bridge (SiS 5511 Chip)

The SiS 5511 chip (PCMC) bridges between the host bus and the PCI local bus. This device integrates cache and memory control functions and provides bus control functions for the transfer of information between the micro-processor, cache, main memory and the PCI bus.

The PCMC monitors each cycle initiated by the CPU, and forwards it to the PCI bus if the CPU cycle does not target the local memory. For the CPU or the PCI to the local memory cycles, the built-in cache and DRAM controller assumes the control to the secondary cache, DRAMs, and the SiS 5512 PCI local data buffer (PLDB).

The main features supported by the PCMC chip are:

- Intel Pentium CPU and CPU at 66/60/50 MHz (external clock speed).
- Integrated PCI bridge (asynchronous PCI clock always @ 33 MHz).
- Host bus frequencies of 50, 60, 66.667 MHz.
- VGA Shared Memory Architecture (with Direct Memory Access):

  Direct Memory Accesses;
  Shared Memory Area 1M and 2M.

- PCI arbiter.
- Pipelined Address Mode of Pentium CPU.
- Integrated Second Level (L2) Cache Controller.
- DRAM Controller, supporting:

  EDO DRAM;
  32-bit/64-bit mix mode.

- Two Programmable Non-Cacheable Regions.
- Option to Disable Local Memory in Non-Cacheable Regions.
- Shadow RAM in Increments of 16 Kbytes.
- Supports SMM Mode of CPU.
- Supports CPU Stop Clock.
- Supports Break Switch.

Feature Summary

Function	Features
Cache controller	❒ 8 bits or 7 bits TAG with Direct mapped organization. ❒ Write back mode (only supported by BIOS) ❒ Uses burst and pipelined burst SRAMs. ❒ 64-KByte to 1 MByte cache summary ❒ Read/Write cycle of 3-1-1-1 using burst or pipelined SRAMS at 66 MHz.
Integrated DRAM controller	❒ Supports four banks of SIMMs. ❒ Supports 256K, 512K, 1MB, 2MB, 4MB, 16MB 70ns FP/EDO DRAM. ❒ Supports 4K refresh DRAM. ❒ Supports 3V or 5V DRAM. ❒ Supports symmetrical and asymmetrical DRAM. ❒ Supports 32 bits/64 bits mixed mode configuration. ❒ Supports concurrent write back. ❒ Supports Read Cycle Power Saving Mode. ❒ Table-free DRAM configuration, auto-detect DRAM size, bank density, single/double sided DRAM, EDO/FP DRAM for each bank. ❒ Supports CAS before RAS “Intelligent Refresh”. ❒ Supports Relocation of System Management Memory. ❒ Optional Parity Checking. ❒ Programmable CAS# Driving Current. ❒ Fully configurable for the Characteristic of Shadow RAM (640 KByte to 1 Mbyte). ❒ Supports EDO/FP 5/6-2-2-2/-3-3-3 burst read cycles.
Integrated PCI Bridge	❒ Supports asynchronous PCI clock. ❒ Translates the CPU cycles into the PCI bus cycles. ❒ Provides CPU-to-PCI Read Assembly and Write Disassembly Mechanism. ❒ Translates sequential CPU-to-PCI Memory Write Cycles into PCI Burst Cycles. ❒ Zero Wait State Burst Cycles. ❒ Provides a prefetch mechanism dedicated for IDE Read. ❒ Supports Advanced Snooping for PCI Master Bursting. ❒ Maximum PCI burst transfer from 256 bytes to 4 Kbytes.
PCI bus arbiter	❒ Supports PCI bus arbitration for up to four masters. ❒ Supports rotating priority mechanism. ❒ Hidden arbitration scheme minimizes arbitration overhead. ❒ Supports concurrence between CPU to memory and PCI to PCI.

Data Path (SiS 5512 Chip)

The SiS 5512 PCI Local Data buffer (PLDB) provides bidirectional data buffering among the 64-bit Host Data Bus, the 64/32-bit Memory Data Bus, and the 32-bit PCI Address/Data Bus.

The PLDB incorporates three FIFOs (First In First Out) and one read buffer among the bridges of the CPU, PCI, and memory buses. This buffering scheme, among many things, smooths the differences in bandwidths between the three buses, therefore improving the overall system performance. During bus operations between the Host, PCI and Memory, the the PLDB receives control signals from the SiS 5511 PCMC, performs functions such as latching data, forwarding data to destination bus, data assemble and disassemble.

The PLDB mainly contains storage elements. The behavior of the Data Path chip is always controlled by the SiS 5511 Host/PCI bridge.

The main features of the SiS 5512 chip are:

- Supports full 64-bit Pentium Processor data bus.
- Provides a 32-bit interface to the PCI.
- Always sustains 0 Wait Performance on CPU-to-Memory.
- Always streams 0 Wait Performance on PCI-to/from-Memory Access.
- Supports built-in 32-bit General Purpose Register.
- Provides parity generation for memory writes.
- Provides optional parity checker for memory reads.

PCI/ISA Bridge (SiS 5513 Chip)

The SiS 5513 chip is a highly integrated PCI/ISA system I/O[1] (PSIO) device that includes all the necessary system control logic used in the PCI/ISA specific applications. The PSIO device serves as a bridge between the PCI bus and the ISA bus, translates ISA master/DMA device cycles onto the PCI bus, and serves as a built-in PCI master/slave IDE interface.

It incorporates a seven-channel programmable DMA controller, 16-level programmable interrupt controller, a programmable timer with three counters with 256 bytes (CMOS SRAM not used), and an onboard Plug and

1. I/O = Input/Out

Play port. The PSIO supports two bus master IDE channels providing up to four IDE devices. The PSIO does not require any IDE buffering to be used, and therefore no IDE buffers are used.

The SiS 5513 chip consists of:

- A PCI bridge that translates PCI cycles onto the ISA bus.
- ISA master/DMA device that translates cycles onto the PCI bus.
- A seven-channel programmable DMA controller.
- A sixteen-level programmable interrupt controller.
- A programmable timer with three counters.
- An onboard Plug and Play port.
- A built-in PCI master/slave IDE interface.

The PSIO PCI bus interface provides the interface between PSIO and the PCI bus. It contains both PCI master and slave bridges to the PCI bus. As a PCI slave, the PSIO responds to both I/O and memory transfers.

ISA Bus Controller

The PSIO ISA Bus Interface accepts cycles from the PCI bus interface and then translates them for the ISA bus. It also requests the PCI master bridge to generate PCI cycles on behalf of DMA or ISA master. The ISA bus interface contains a standard ISA Bus Controller and a Data Buffering logic. The PSIO can directly support six ISA slots without external data or address buffering.

DMA Controller

The PSIO contains a seven-channel DMA controller. The channel 0 to 3 is for 8-bit DMA devices while channel 5 to 7 is for 16-bit devices. The channels can also be programmed for any of the four transfer modes: The three active modes (single, demand, block), can perform three different types of transfer: read, write and verify. The address generation circuitry in the PSIO can only support a 24-bit address for DMA devices.

Interrupt Controller

The PSIO provides an ISA-compatible interrupt controller that incorporates the functionality of two 82C59 interrupt controllers. The two controllers are cascaded so that 14 external and two internal interrupts are supported.

Timer/Counter

The PSIO contains a three-channel counter/timer. The counters use a division of 14.31818 MHz OSC input as the clock source.

System Board Switches and Jumpers (D4051-63001)

The system board switches and jumpers are used to configure certain aspects of the computer.

SW1 Switch

This switch is multi-purpose and is used to modify Flash, CMOS and password settings.

Switch	Default Setting	OFF	ON	COMMENTS
1	OFF	Flashing Enable	Flashing Disable	Updating the BIOS. Set the security mode. Set the switch to the ON position to prevent the BIOS from being upgraded.
2	OFF	CMOS is in normal operation	CMOS Clear	To clear the CMOS configuration. Set the switch to the ON position and restart the PC. Return the switch to the OFF position and restart the PC to return to normal operation.
3	OFF	Password is in normal operation	Password Clear	To clear the password. Set the switch to the ON position and restart the PC. Return the switch to the OFF position and restart the PC to return to normal operation.

SW2 Switch

This switch is used to select the internal CPU frequency by defining the CPU Bus Frequency / CPU Frequency ratio. If the processor is upgraded, the ratio might have to be changed to adapt to the new processor.

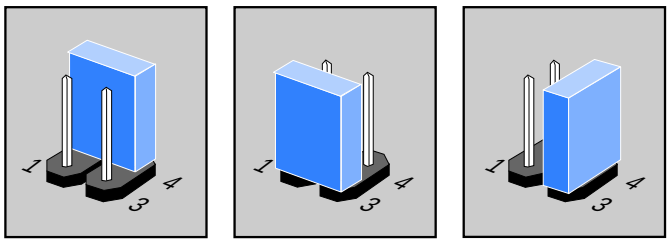
The following table includes some examples of the settings to use for different processor speeds:

Processor Speeds	Switch Block SW2 Position			Jumper J7 Settings	
	Ratio	1	2	CPU Bus Frequency	Pins Shorted
CPU Frequency 100 MHz	2 / 3	OFF	OFF	66 MHz	3 - 4
CPU Frequency 120 MHz	1 / 2	ON	OFF	60 MHz	1 - 3
CPU Frequency 133 MHz	1 / 2	ON	OFF	66 MHz	3 - 4
CPU Frequency 150 MHz	2 / 5	ON	ON	60 MHz	1 - 3
CPU Frequency 166 MHz	2 / 5	ON	ON	66 MHz	3 - 4

The default settings for Switch 2 and Jumper J7 depend on the particular HP Vectra 500 Series PC model.

CPU Bus Frequency Jumper

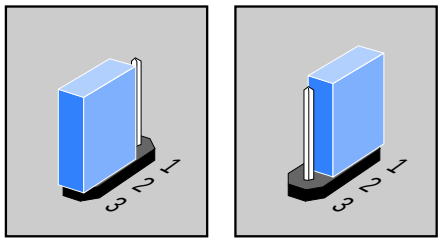
This jumper (J7) defines the CPU bus frequency. The following illustration shows how to set the desired bus frequency.



50 MHz 60 MHz 66 MHz

Cache Jumper

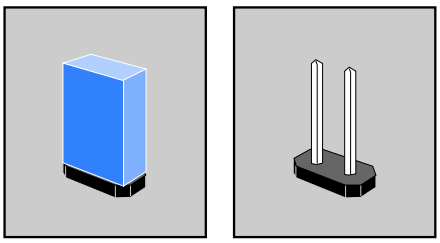
This jumper (J6) selects either synchronous or asynchronous cache type. If the PC is not installed with any level-2 cache, the default jumper setting is synchronous cache. The following illustration shows the two cache-type jumper settings.



Synchronous Asynchronous

Space-Bar Power-On Feature Jumper

The Space-Bar Power-On feature (JP4 “KBD Start” on the system board) enables you to turn on the PC using the spacebar. To disable this feature, set the Space-Bar Power-On field in the *Setup* program to Disable, or remove the jumper. Removing the jumper overrides the setting in the *Setup* program.



Power-on spacebar enabled | Power-on spacebar disabled

NOTE:

To use the Power-On spacebar feature, an HP Vectra Keyboard displaying a Power-On icon is required.

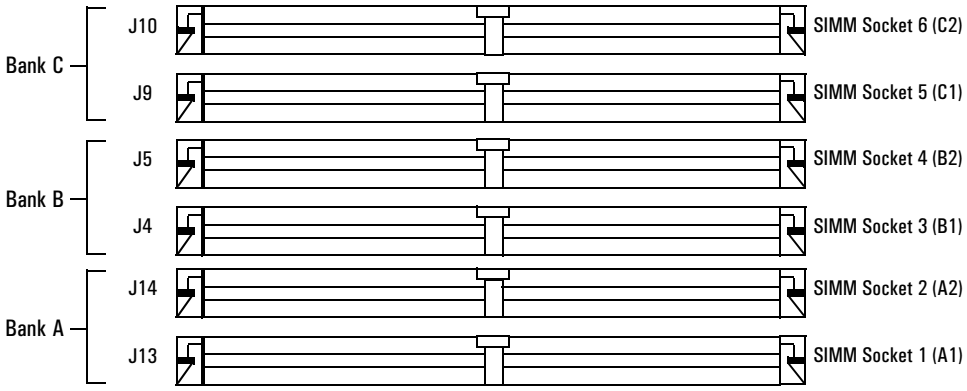
Processor Socket (D4051-63001)

The microprocessor is packaged in a pin-grid-array (PGA), which is seated on the system board in a zero-insertion-force (ZIF) socket.

Memory Sockets (D4051-63001)

There are six main memory module sockets available with the HP Vectra 500 Series minitower and desktop computers. The sockets are arranged in three banks (A to C), allowing memory installation up to a maximum of 192 MB.

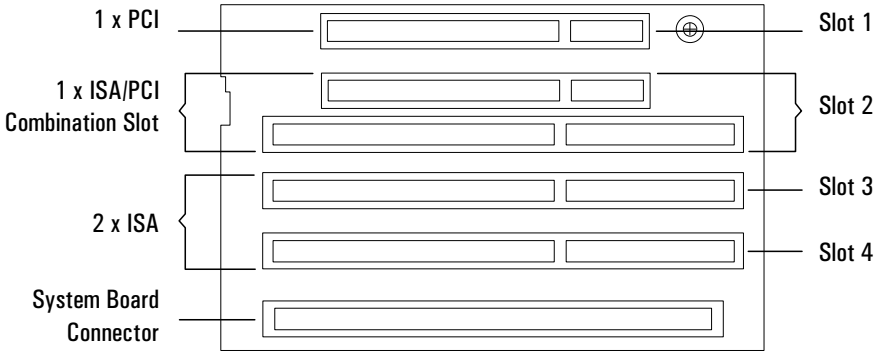
The following illustration shows the physical layout of the memory bank organization.



Backplane (D4051-63001)

Desktop Backplane

The HP Vectra 500 Series desktop backplane supports two 16-bit ISA (Industry Standard Architecture) cards, one 32-bit PCI (Peripheral Component Interconnect) card and has one combination slot for an ISA or PCI card.

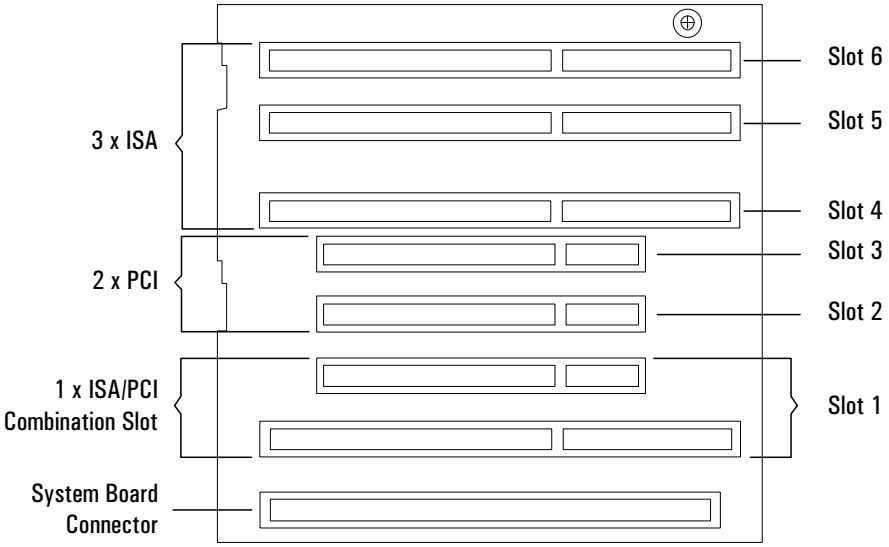


The four expansion card slots are arranged as follows:

- Slot 1 - (the top slot) can be used for a 32-bit PCI card.
- Slot 2 - Combination slot that can be used for a 32-bit PCI card or a full-length (30 cm / 12 inches) 16-bit ISA card.
- Slot 3 - can be used for a full-length 16-bit ISA card (30 cm / 12 inches).
- Slot 4 - can be used for a half-length 16-bit ISA card (15 cm / 6 inches).

Minitower Backplane

The HP Vectra 500 Series minitower backplane supports three 16-bit ISA (Industry Standard Architecture) cards, two 32-bit PCI (Peripheral Component Interconnect) cards and has one combination slot for an ISA or PCI card.



The six expansion card slots are arranged as follows:

- Slot 1 - (the innermost) Combination slot that can be used for a half-length 16-bit ISA card (15 cm / 6 inches) or a 32-bit PCI card.
- Slot 2 - can be used for a 32-bit PCI card.
- Slot 3 - can be used for a 32-bit PCI card.
- Slot 4 - can be used for a full-length 16-bit ISA card (30 cm / 12 inches).
- Slot 5 - can be used for a full-length 16-bit ISA card (30 cm / 12 inches).
- Slot 6 - can be used for a full-length 16-bit ISA card (30 cm / 12 inches).

Devices on the Processor Local Bus (D4051-63001)

Main Memory (UMA)

The SiS 5511 chip can support single-sided or double-sided 64/72 bits (with or without parity) FP (Fast Page mode) or EDO (Extended Data Output) DRAM (dynamic random-access memory) modules. Half populated banks are also supported. The PC can use 60 ns EDO or 70 ns FP DRAM.

It is also possible to mix the EDO DRAM and FP DRAM bank by bank and the corresponding DRAM timing will be switched automatically according to register setting. Both symmetrical and asymmetrical type DRAMs are supported.

The following table is an example of how to use the memory module banks, with three different configurations.

	BANK A		BANK B		BANK C	
Memory Total	**A1**	**A2**	**B1**	**B2**	**C1**	**C2**
8 MB	4 MB	4 MB				
12 MB	4 MB	4 MB	4MB			
16 MB	8 MB	8 MB				

Cache Memory (D4051-63001)

The PC supports two levels of cache memory:

- Level-1 (L1), cache memory which is incorporated within the Pentium processor chip.
- Level-2 (L2), cache memory which is optionally installed as a memory module on the system board.

Cache memory acts as temporary storage for data and instructions from main memory. Since the system is likely to use the same data several times, it is faster to get it from the on-chip cache than from the main memory.

Level-1 Cache Memory

The L1 cache memory is divided into two separate banks:

- L1 I-cache for instruction words.
- L1 D-cache for data words.

For more information about Level-1 cache, refer to “Instruction and Data Cache” on page 46.

Level-2 Cache Memory

The L2 cache memory, when installed, has a 32-byte line size. It is controlled by the Host Bridge chip (SiS 5511) in the system board chipset. A single HP cache memory module consists of 256 KB of direct mapped, synchronous, static random access memory (SRAM).

Pentium Processor (D4051-63001)

The Pentium processor uses 64-bit architecture and is 100% compatible with Intel’s family of x86 processors. All application software that has been written for Intel386 and Intel486 processors can run on the Pentium without modification. The Pentium processor contains all the features of the Intel486 processor, with the following added features which enhance performance:

- Superscalar Architecture
- Floating Point Unit
- Dynamic Branch Prediction
- Instruction and Data cache
- Data Integrity
- Supports MultiProcessor Specification (MPS) 1.1
- PCI bus architecture
- Advanced Power Management capability for reducing power consumption

The processor is seated in a Zero Insertion Force (ZIF) socket.

Superscalar Architecture

The Pentium processor's superscalar architecture has two instruction pipelines and a floating-point unit, each capable of independent operation. The two pipelines allow the Pentium to execute two integer instructions in parallel, in a single clock cycle. Using the pipelines halves the instruction execution time and almost doubles the performance of the processor, compared with an Intel486 microprocessor of the same frequency.

Frequently, the microprocessor can issue two instructions at once (one instruction to each pipeline). This is called instruction pairing. Each instruction must be simple. One pipeline will always receive the next sequential instruction of the one issued to the other pipeline.

Floating Point Unit

The Floating Point Unit (FPU) incorporates optimized algorithms and dedicated hardware for multiply, divide, and add functions. This increases the processing speed of common operations by a factor of three.

Dynamic Branch Prediction

The Pentium processor uses dynamic branch prediction. To dynamically predict instruction branches, the processor uses two prefetch buffers. One buffer is used to prefetch code in a linear way, the other to prefetch code depending on the contents of the Branch Target Buffer (BTB). The BTB is a small cache which keeps a record of the last instruction and address used. It uses this information to predict the way that the instruction will branch the next time it is used. When it has made a correct prediction, the branch is executed without delay, thereby enhancing performance.

Instruction and Data Cache

The Pentium processor has separate on-chip code instruction and data caches. Each cache is 8 KB in size with a 32-bit line. The cache acts as temporary storage for data and instructions from the main memory. As the system is likely to use the same data several times, it is faster to get it from the on-chip cache than from the main memory.

Each cache has a dedicated Translation Lookaside Buffer (TLB). The TLB is a cache of the most recently accessed memory pages. The data cache is configured to be Write-Back on a line-by-line basis (a line is an area of memory of a fixed size).

The data cache tags (directory entries used to reference cached memory pages) are triple-ported to support two data transfers and an inquire cycle in the same clock cycle. The code cache tags are also triple-ported to support snooping (a way of tracking accesses to main memory by other devices) and split line accesses.

Individual pages of memory can be configured as cacheable or non-cacheable by software or hardware. They can also be enabled and disabled by hardware or software.

Data Integrity

The processor uses a number of techniques to maintain data integrity. It employs two methods of error detection:

- Data Parity Checking

  This is supported on a byte-by-byte basis, generating parity bits for data addresses sent out of the microprocessor. These parity bits are not used by the external subsystems.

- Internally

  The processor uses functional redundancy checking to provide maximum error detection of the processor and its interface.

Advanced Power Management

The Advanced Power Management (APM) is a standard, defined by Intel and Microsoft, for a power-saving mode that is applicable under a wide range of operating systems. The version APM 1.1 supports the following modes: *Fully-on, Standby, Suspend*, and *Off*.

The *Suspend* mode is managed at the operating system level only, from the Windows 95 Start menu. There is no longer the inter-activity between BIOS *Setup* and operating systems, and no longer a “sleep at” item on the *Setup* program menus, to avoid the BIOS from shutting down the system at the wrong moment.

Devices on the PCI Bus

Graphics/Integrated Video (D4051-63001)

The HP Vectra 500 Series PC uses the SiS 6205 video controller and supports video resolutions up to 1280 x 1024.

Video Controller

As explained earlier, the SiS 6205 video controller supports the UMA architecture, and therefore no dedicated video memory is loaded on the system board. The shared frame buffer is located in the system DRAM, and the video controller accesses it through the M A (MA) and M D (MD) bus. The SiS 6205 video controller arbitrates for the use of the system memory with the memory controller included in the SiS 5511 Host Bridge and Memory Controller. Whenever the video controller wants to access the memory bus, it makes a request to the SiS 5511 controller. This then grants the memory bus to the SiS 6205 video controller unless it is needed by the chipset. The arbitration scheme takes place through three signals: VGAREQ#, VGAGNT#, and PREQ (if the high/low priority scheme is enabled).

The SIS 6205 video controller offers full compatibility with VGA. In addition, the features are enhanced beyond Super VGA by hardware which accelerates graphical user interface operation in Windows 95.

The enhanced features include:

- Direct connectivity to PCI bus.
- True acceleration for 8, 16 and 32-bit pixel depths.
- 57 MHz clock for video memory.
- Fully programmable Pixel Clock Generator up to 135 MHz.
- Fast linear addressing with full software relocation.

For details about supported video resolutions, refer to “Video Controllers” on page 115 for a table containing all the video resolutions supported.

Integrated Drive Electronics (IDE) Controller

The IDE controller is implemented as part of the PCI/ISA bridge chip. It is driven from the PCI bus and has PCI-Master capability. It supports Enhanced IDE (EIDE) and Standard IDE (Bus Master IDE). To use the Enhanced IDE features, though, hard disk drives must be compliant with Enhanced IDE.

The following table shows the two different cable sets for the desktop and minitower computers.

	Desktop	Minitower
The first cable attached to the connector marked HDD on the system board, supports:	Up to two IDE hard disk drives	Up to two IDE hard disk drives
The second cable attached to the connector marked CD-ROM on the system board, supports:	Either an IDE CD-ROM drive or an IDE hard disk drive	An IDE CD-ROM drive and a third hard disk drive, or two IDE CD-ROM drives

The following tables show the possible multiple IDE drive combinations for the desktop and minitower computers when installing additional devices.

Desktop	Configuration	Connections to Data Cables	
	One hard disk drive	1. Bootable hard disk drive:	Master connector, HDD data cable
	Two hard disk drives	1. Bootable hard disk drive: 2. Second hard disk drive:	Master connector, HDD data cable Slave connector, HDD data cable
	Three hard disk drives	1. Bootable hard disk drive: 2. Second hard disk drive: 3. Third hard disk drive:	Master connector, HDD data cable Slave connector, HDD data cable Master connector, CD-ROM data cable
	One hard disk drive One CD-ROM drive	1. Bootable hard disk drive: 2. CD-ROM drive:	Master connector, HDD data cable Master connector, CD-ROM data cable
	Two hard disk drives One CD-ROM drive	1. Bootable hard disk drive: 2. Second hard disk drive: 3. CD-ROM drive:	Master connector, HDD data cable Slave connector, HDD data cable Master connector, CD-ROM data cable

Minitower	Configuration	Connections to Data Cables
	One hard disk drive	1. Bootable hard disk drive: Master connector, HDD data cable
	Two hard disk drives	1. Bootable hard disk drive: Master connector, HDD data cable 2. Second hard disk drive: Slave connector, HDD data cable
	Three hard disk drives	1. Bootable hard disk drive: Master connector, HDD data cable 2. Second hard disk drive: Slave connector, HDD data cable 3. Third hard disk drive: Master connector, CD-ROM data cable
	One hard disk drive One CD-ROM drive	1. Bootable hard disk drive: Master connector, HDD data cable 2. CD-ROM drive: Master connector, CD-ROM data cable
	Two hard disk drives One CD-ROM drive	1. Bootable hard disk drive: Master connector, HDD data cable 2. Second hard disk drive: Slave connector, HDD data cable 3. CD-ROM drive: Master connector, CD-ROM data cable
	Three hard disk drives One CD-ROM drive	1. Bootable hard disk drive: Master connector, HDD data cable 2. Second hard disk drive: Slave connector, HDD data cable 3. Third hard disk drive: Master connector, CD-ROM data cable 4. CD-ROM drive: Slave connector, CD-ROM data cable
	Two hard disk drives Two CD-ROM drives	1. Bootable hard disk drive: Master connector, HDD data cable 2. Second hard disk drive: Slave connector, HDD data cable 3. CD-ROM driver: Master connector, CD-ROM data cable 4. Second CD-ROM drive: Slave connector, CD-ROM data cable

The BIOS uses the auto-detected drive information to select the fastest configuration supported by each installed IDE drive.

Transfer Rates Versus Modes of Operation

The IDE controller supports 32-bit Windows and DOS I/O transfers (many IDE controllers use Windows integral IDE driver which only supports 16-bit I/O transfers). It supports programmed I/O (PIO) modes up to mode 4 and direct memory access (DMA) modes up to mode 2 (giving a cycle time of 120 ns, and a transfer rate of 16.7 MB per second, in both cases).

The five PIO modes allow the following transfer rates:

Mode	0	1	2	3	4
Cycle time (ns)	600	383	240	180	120
Transfer rate (MBytes/s)	3.33	5.22	8.33	11.1	16.7

The three DMA modes allow the following transfer rates:

Mode	0	1	2
Cycle time (ns)	480	150	120
Transfer rate (MBytes/s)	4.2	13.3	16.7

Operated in slave mode, the IDE controller saturates the PCI bus with transfers, thus limiting the actual achieved transfer rate to less than 10 MBytes per second.

Operated in master mode, though, the IDE controller is allowed to work autonomously of the processor, and the full 16.7 MBytes per second transfer rate can be achieved with less than 33% occupancy of the PCI bus (thus allowing the processor to do other work for more than 67% of the cycle times, while the IDE transfers take place in parallel).

Disk Capacity Versus Modes of Addressing

The amount of addressable space on the hard disk is limited by three factors:

- Physical size of the hard disk.
- Addressing limit of the IDE hardware.
- Addressing limit of the BIOS.

The Extended-CHS (Cylinder Header Sector) addressing scheme allows larger disk capacities to be addressed than under CHS, by performing a translation (for example regrouping the sectors so that there are twice as many logical tracks as is possible under the CHS addressing scheme).

	Cylinders per Device	Heads per Cylinder	Sectors per Track	Bytes per Sector	Bytes per Device
CHS	64	16	1024	512	528 M
ECHS	64	256	1024	512	8.4 G
LBA	-	-	256 M ($=2^{28}$)	512	137 G

If the *Setup* field has been set to **`automatic`**, the logical block addressing (LBA) mode will be selected for each device that supports it.

Devices on the ISA Bus

Super I/O Chip (NS 87308 or NS 87307)

The basic input/output control functions are provided by the Super I/O chip, the NS 87308 or NS 87307. The Super I/O chip is contained within a 160-pin PQFP package. The chip provides the control for the following devices:

Logical Device	Functions
0	Keyboard controller
1	Mouse controller
2	RTC and Advanced Power supply Controller (APC)
3	Floppy disk controller
4	Parallel port controller
5	UART2 & IR controller
6	UART1 controller
7	GPIO
8	Power management

The Super I/O chip incorporates one Plug and Play compatible chip, is 100% compatible with the ISA architecture, and provides:

- An integrated floppy drive controller.
- A keyboard controller.
- A mouse controller.
- A real-time clock (RTC).
- Two UART's (serial ports).
- An IEEE1284 parallel port.
- Three general purpose chip select signals
- General purpose I/O register set.
- An X-bus data buffer that connects the 8-bit X data bus to the ISA data bus.
- Non-Volatile Memory (NVM) support via the Chip Select 0 (CS0) signal that is powered by the V_{CCH}.

Feature Summary

Function	Features
Floppy disk controller	❒ Software compatible with the DP8473, the 765A, and the N82077 ❒ 16-byte FIFO (default disabled) ❒ Burst and non-burst modes ❒ Perpendicular recording drive support ❒ New high-performance internal digital data separator (no external filter components required) ❒ Low-power CMOS with enhanced power-down mode ❒ Automatic media-sense support
UARTs	❒ Software compatible with the PC16550A and PC16450 ❒ A modifiable address that is referenced by a 16-bit programmable register. ❒ 13 IRQ channel options. ❒ Shadow register support for write-only bits. ❒ Four 8-bit DMA options for UART2.
Bidirectional parallel port	❒ Enhanced Parallel Port (EPP) compatible ❒ Extended Capabilities Port (ECP) compatible ❒ Bidirectional under either software or hardware control ❒ Demand mode DMA support. ❒ Selection of internal pull-up or pull-down resistor for Paper End (PE) pin. ❒ Reduction of PCI bus utilization by supporting a demand DMA mode mechanism and a DMA fairness mechanism. ❒ Includes protection circuit against damage caused when printer is switched on, or operated at higher voltages. ❒ Output buffers that can sink and source 14 mA.
Three general purpose pins for three separate chip select signals	❒ Programmed for game port control. ❒ Chip Select 0 (CS0) signal produces open drain and is powered by the V_{CCH}. ❒ Chip Select 1 (CS1) and 2 (CS2) signals have push-pull buffers and are powered by the main V_{DD}. ❒ Decoding of chip select signals depends on the address and the Address Enable (AEN) signal, and can be qualified using the Read (RD) and Write (WR) signals.
Enhanced power management	❒ Special configuration registers for power down ❒ Reduced current leakage from pins. ❒ Low-power CMOS technology. ❒ Ability to shut off clocks to all modules.

Function	Features
16 Single-Bit General Purpose I/O ports (GPIO)	❒ Modifiable addresses that are referenced by a 16-bit programmable register. ❒ Programmable direction for each signal (input or output). ❒ Programmable drive type for each output pin (open-drain or push-pull). ❒ Programmable option for internal pull-up resistor on each input pin. ❒ A back-drive protection circuit.
Clock source options	❒ Source is a 32.768 kHz crystal (an internal frequency multiplier generates all the required internal frequencies). ❒ Source may be either a 48 MHz or 24 MHz clock input signal.
General features	❒ All accesses to the Super I/O chip activates a Zero Wait State (ZWS) signal, except for accesses to the Enhanced Parallel Port (EPP) and to configuration registers. ❒ Accesses to all configuration registers is through an Index and a Data register, which can be relocated within the ISA I/O address space. ❒ 160-pin Plastic Quad Flatpack (PQFP) package.

Serial/Parallel Ports

The Super I/O chip supports two serial ports and one bidirectional parallel port. The serial ports are high speed UARTs with 16-Byte FIFOs, and can be programmed as COM1, COM2, COM3, COM4, or disabled.

The parallel port can operate in four modes:

- Standard mode (PC/XT, PC/AT, and PS/2 compatible)
- Bidirectional mode (PC/XT, PC/AT, and PS/2 compatible)
- Enhanced mode (Enhanced Parallel Port or EPP compatible)
- High speed mode (MS/HP Extended Capabilities Port or ECP compatible).

  It can be programmed as LPT1 (378h, IRQ7), LPT2 (278h, IRQ5), or disabled.

Floppy Drive Controller

The Floppy Drive Controller (FDC) is software and register compatible with the 82077AA, and 100% IBM compatible. It has an A and B drive-swapping capability and a non-burst DMA option. The FDC supports any combination of the following: tape drives, 3.5 inch flexible disk drives, 5.25 inch flexible disk drives.

Keyboard and Mouse Controller

The PC has an 8042-based keyboard and mouse controller (the socket pin layouts are as shown on page 24). The C3758A keyboard is supplied for use with the Windows 95 operating system (though it will also work with other operating systems). It has the following capabilities:

- Space-bar power-on, to start the computer from the *Off* state (if **`power on from keyboard`** is enabled in the *Setup* program).
- Windows key (next to the Alt keys), which has the same effect as clicking the Start button on the Windows 95 task bar.
- Pull-down key (next to the right Ctrl key), which has the same effect as clicking the right mouse button.

BIOS (version: GX.07.xx)

The following section is an overview of the BIOS features available with the system identified by the BIOS version: GX.07.xx, installed on the HP Vectra 500 Series PC models with an HP Service Part Number: D4051-63001. For further detailed information about the BIOS, refer to chapter 4, Summary of the HP/Phoenix BIOS.

HP *Setup* Program

The PC has many security features to protect stored data, to protect the SETUP configuration, and to prevent unauthorized operation of software applications:

- User password.
- Administrator password (system configuration protection).
- Power-on prompt, with user or administrator password.
- Space-bar power-on protection. (Feature may be enabled or disabled.)
- Communications port protection. (Ports can enabled or disabled.)
- Floppy disk drive protection. (Disks can be read- or write-protected.)
- Boot protection. (Boot on floppy disk , CD-ROM and hard disk can be enabled or disabled).

Flash ROM

The PC uses 256 KB of 200ns, Flash ROM. The HP BIOS boot code contains SETUP, video BIOS, error messages, and ISA and PCI initialization. During programming of the Flash ROM, the power supply switch and the reset button are disabled to prevent accidental interruption.

Little Ben

Little Ben is an HP application specific integrated circuit (ASIC) that is connected between the chipset and the processor. It has been designed to act as a companion to the Super I/O chip.

3

System Board (P/Ns D3657-63001 and D3661-63001)

The two system boards described in this chapter use the Intel SB82437/8 PCI chipset. The two boards are the same except that D3657-63001 has an integrated (onboard) video controller and memory, whereas D3661-63001 uses a Matrox Millennium video card for its video controller and memory.

Overview

This section lists the 520 and 525 models and product numbers that use the two system boards D3657-63001 and D3661-63001.

D3657-63001 Models

Desktop Models

The following table lists the desktop models and products that use the D3657-63001 system board.

Model	Product Number	
520 MCx2 5/133	D4479A	
520 MCx2 5/166	D4480A	
1 = Includes CD-ROM 2 = Includes CD-ROM and Modem/Audio		

Minitower Models

The following table lists the minitower models and products that use the D3657-63001 system board.

Model	Product Number		
525 5/166	D4483A		
525 5/200	D4474A		
525 CD1 5/133	D4475A		
525 CD1 5/166	D4476A		
525 CD1 5/200	D4470A	D4472A	
525 MCx2 5/133	D4477A		
525 MCx2 5/166	D4478A		
525 MCx2 5/200	D4473A	D4481A	D4482A
1 = Includes CD-ROM 2 = Includes CD-ROM and Modem/Audio			

D3661-63001 Models

Minitower Models

The following table lists the minitower models and products that use the D3661-63001 system board.

Model	Product Number	
525 MCx2 5/200	D4471A	

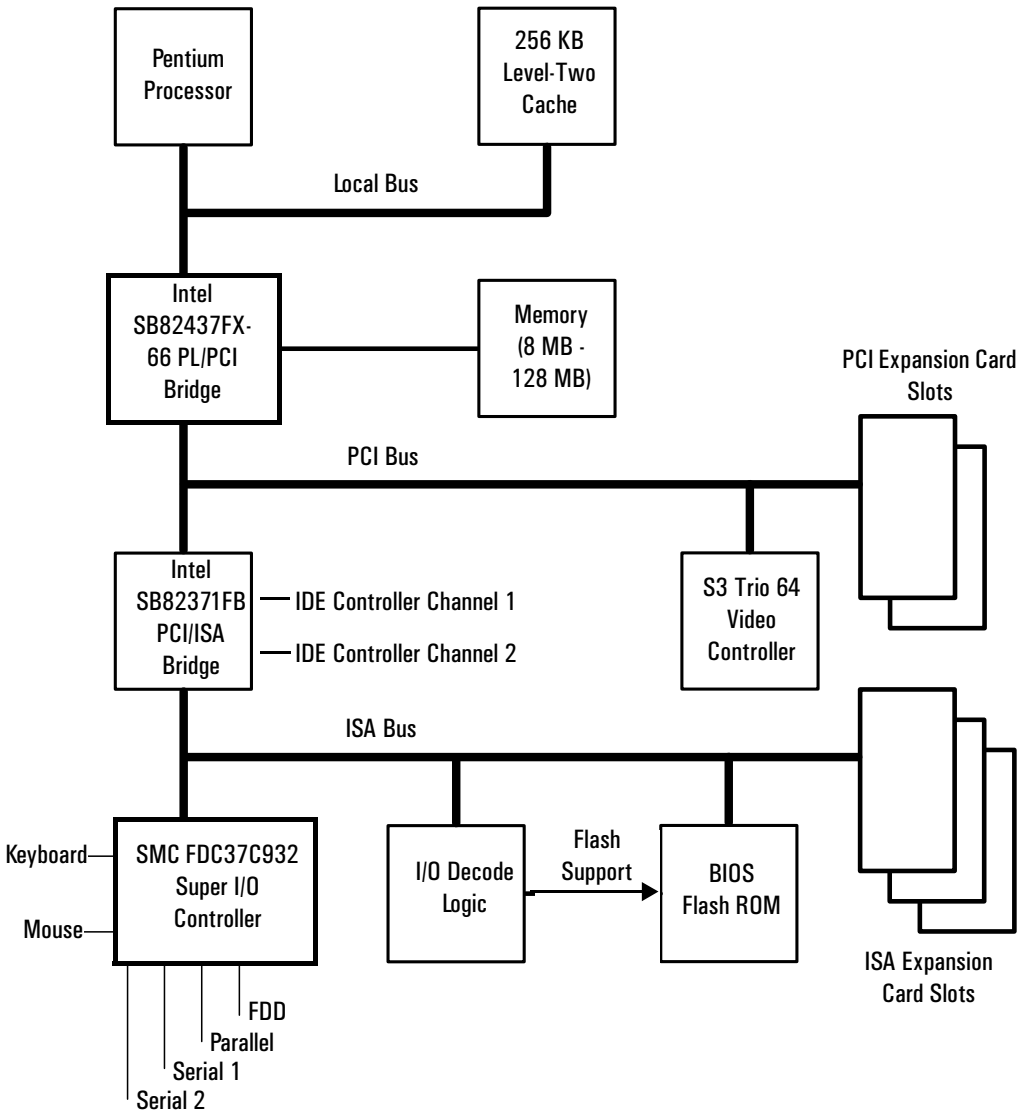
1 = Includes CD-ROM
2 = Includes CD-ROM and Modem/Audio

Configuration Summary

- Supported processors: P54C and P54CS.
- Level-2 cache memory socket - supports 256-KB cache memory module (the module is already installed in some PCs).
- Intel SB82437/8 PCI chipset which consists of four chips that interface between the three main buses (the processor's local (PL) bus, the PCI bus, and the ISA bus).
  - ❒ The PL/PCI bridge chip (SB82437FX-66) which also provides control for the PCI bus, level-2 cache memory, and main memory.
  - ❒ Two data path unit chips (SB82438FX) that provide a 64-bit data path between the processor local bus and main memory modules.
  - ❒ The PCI/ISA bridge chip (SB82371FB) which also provides control for the IDE.
- Six SIMM sockets for EDO or FPM DRAM - up to 128 MB.
- Onboard video controller (S3 Trio64) offers full compatibility with VGA. Note that one model (D4471A) uses a Matrox MGA Millennium video card instead of the onboard video controller.
- Super I/O controller (SMC FDC37C932), driven from the ISA bus, supports two serial ports and one bidirectional multi-mode parallel port. It also provides control for two slow mass-storage devices (any suitable combination of floppy disk and tape drives).
- Little-Ben chip which takes care of security features and power management.
- 128-KB flash BIOS

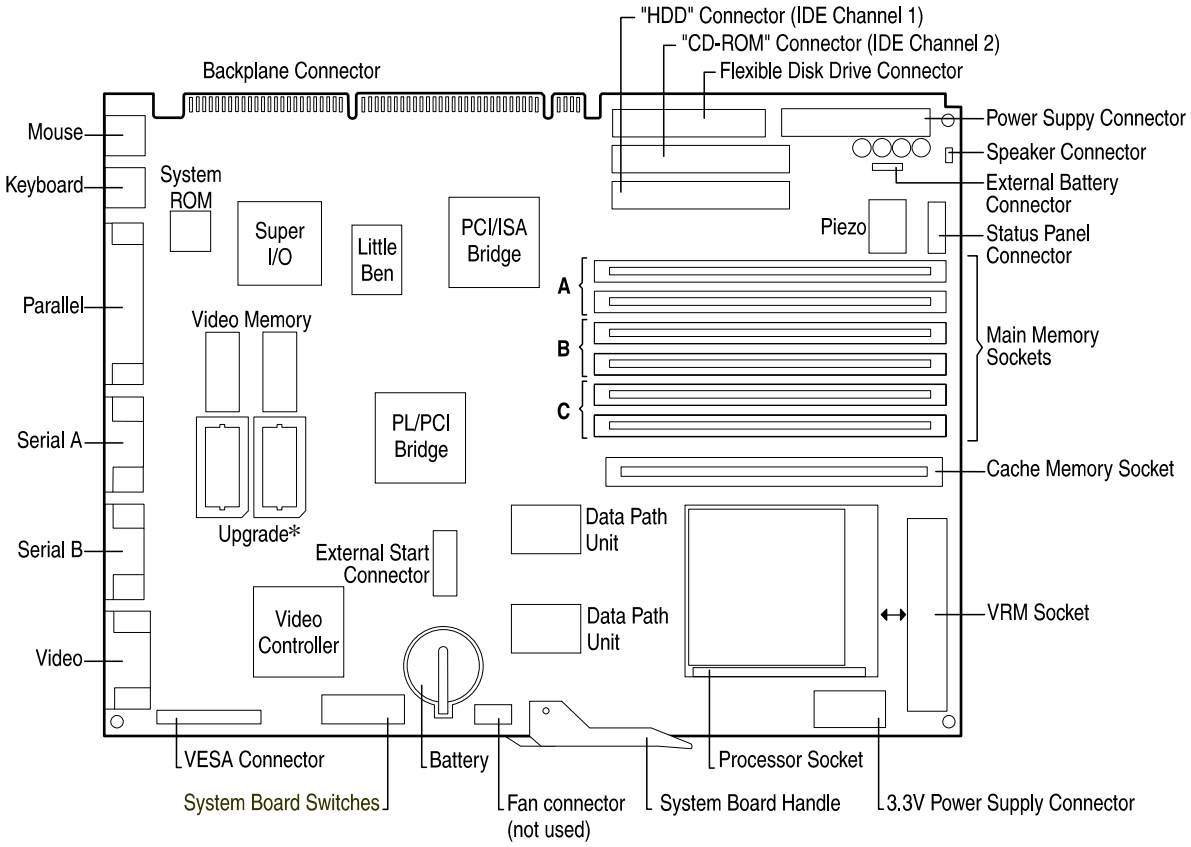
System Board Architecture

The following diagram shows the functional relationship between the various components on the system board.



System Board Physical Layout

The following diagram shows the physical layout of the system board.



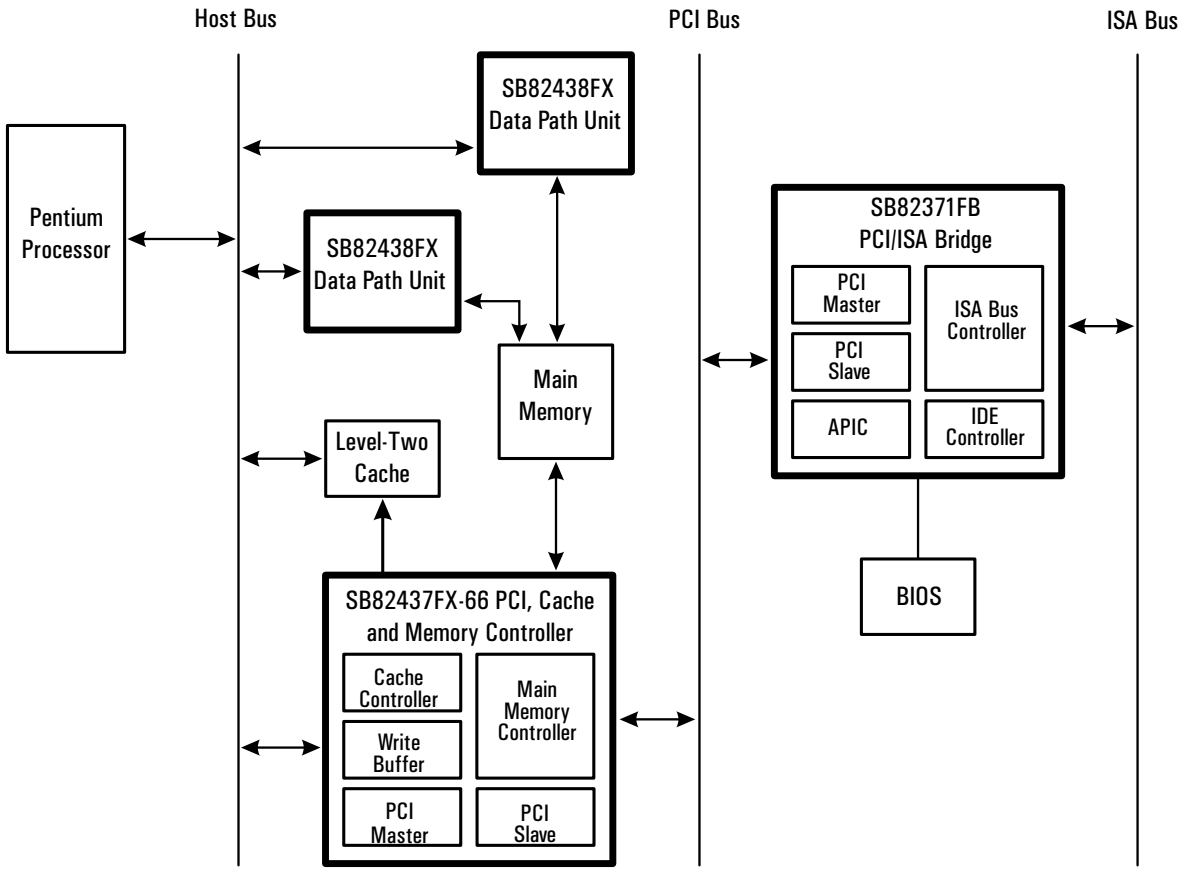
* This video upgrade applies only to the models with integrated video controller.

Principal Components and Features

PCI Chipset

The PCI chipset consists of four chips that interface between the three main buses (the processor's local (PL) bus, the PCI bus, and the ISA bus):

- The PL/PCI bridge chip (SB82437FX-66) which also provides control for the PCI bus, level-2 cache memory, and main memory.
- Two data path unit chips (SB82438FX) that provide a 64-bit data path between the processor local bus and main memory modules.
- The PCI/ISA bridge chip (SB82371FB) also provides control for the IDE.



PCI, Cache and Memory Controller (SB82437FX-66)

The SB82437FX-66 device integrates cache and memory control functions and provides bus control functions for the transfer of information between the microprocessor, cache, main memory and the PCI bus. The cache controller supports the Pentium Cache Write-Back mode and 256 KB of direct mapped, write-back level-two cache, using synchronous pipeline burst SRAMs.

SB82437FX-66 Feature Summary

Function	Features
Cache controller	❒ Direct mapped organization ❒ Buffered write-back ❒ External cache tags ❒ 32-byte line size ❒ Uses synchronous pipeline burst SRAM ❒ Supports 3-1-1-1[1] burst reads
Write buffer	❒ Buffers all processor writes to main memory ❒ Buffers memory writes to PCI for selected memory regions ❒ Supports 3-1-1-1[1] write access timing
DRAM controller	❒ Uses dedicated DRAM memory address and data buses ❒ Page mode - one or two pages open simultaneously ❒ Supports pipelined accesses ❒ Full RAS/CAS programmability ❒ Flexible bank configurations (each bank programmable for DRAM size, bank width and single or double-sided modules) ❒ Self configuring bank start addresses ❒ Shadow RAM support for the memory region 640 KB - 1 MB (in 16-KB segments) ❒ System management memory support ❒ RAS only refresh ❒ Fast memory access 7-2-2-2[1] with Extended Data Out (EDO) memory
PCI slave interface	❒ Becomes processor (local) bus master to generate DRAM requests on behalf of other PCI bus masters ❒ Supports PCI bus burst cycles ❒ Supports posted writes to DRAM for PCI burst writes ❒ Supports read-ahead from DRAM for PCI burst reads

Function	Features
PCI master interface	❒ Provides for programmable PCI bus memory regions in memory address map ❒ Supports PCI bus burst cycles for 64-bit and 32-bit misaligned Pentium reads and writes ❒ Optional posting of PCI memory and I/O writes ❒ Optional buffering of PCI memory writes ❒ Optional read-ahead for processor to PCI accesses
PCI bus arbiter	❒ Supports PCI bus arbitration for up to four masters ❒ Supports rotating priority scheme

[1] The Pentium's internal cache has a 32-byte line size, which is four times the width of the Pentium's host data bus. Burst reads and writes by the Pentium involve a full cache line, and so require four back-to-back cycles to complete. The first cycle in each burst of four always requires more time to complete than the three subsequent cycles. This is because the first cycle includes the addressing phase and precharge timing (for memory).

Data Path Unit (SB82438FX)

The SB82438FX component contains a 64-bit data path between the host bus and main memory. A 4×64-bit deep buffer provides 3-1-1-1 writes to main memory.

This buffer is used for:

- writes from processor to main memory
- level-two cache write-back cycles
- transfers from PCI to main memory.

The PCI/ISA Bridge and IDE Controller (SB82371FB)

The SB82371FB device serves as a bridge between the PCI bus and the ISA expansion bus, and incorporates a two-channel PCI IDE controller. It incorporates the logic for a PCI interface, a DMA interface, a DMA controller that supports fast DMA transfers, data buffers to isolate the PCI and ISA buses, Timer/Counter logic, and NMI control logic.

The SB82371FB PCI/ISA bridge also provides decode for the following peripheral devices:

- Flash BIOS
- Real Time Clock/CMOS Memory
- Keyboard/Mouse Controller
- Floppy Disk Controller
- Two Serial Ports
- One Parallel Port
- PCI Expansion Card Slots.

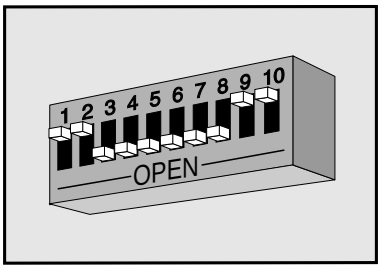
The SB82438FX and SB82371FB Feature Summary

Function	Features
Data buffer (for SB82438FX and SB82371FB together)	❒ Provides a high performance 64-bit data path between the processor (local) bus and main memory ❒ Provides a 32-bit data path to the PCI bus ❒ Provides a 8-deep x 64-bits wide write buffer for all processor writes to main memory ❒ Provides a one-level posted write buffer for all processor writes to PCI bus memory
PCI master / slave interface (for SB82371FB only)	❒ Fully compatible with PCI specification ❒ Supports PCI-to-ISA / ISA-to-PCI bus master cycle translations ❒ Supports programmable memory regions to provide fast positive decode for PCI master accesses ❒ Implements subtractive decoding for unclaimed PCI cycles ❒ Supports PCI-to-ISA posted memory writes ❒ Translates DMA transfers for PCI slaves ❒ Supports PCI address/data parity generation and checking

Function	Features
ISA bus controller (for SB82371FB only)	❒ Fully compatible with ISA bus standard ❒ Supports asynchronous ISA bus operation up to 16 MHz ❒ Integrates: ❒ two 82C37A DMA controllers ❒ two 82C59A interrupt controllers ❒ 82C54 timer ❒ hidden ISA refresh controller ❒ support for BIOS ❒ port A, B and NMI logic
Fast IDE controller (for SB82371FB only)	❒ Supports PIO and Bus Master IDE ❒ Supports up to Mode 4 timings ❒ Up to 22 MB/s transfer rate ❒ 8×32-bit buffer for Bus Master IDE PCI burst transfers

System Board Configuration Switches

The system board configuration switches are used to configure certain aspects of the computer.



Example of system board switch settings

The system board switches used for configuring the PC are summarized in the following table.

Switch	Setting	Switch Functions	Default Setting
1 - 4	-	Selects system board speed settings, refer to "Bus Frequencies" on page 72.	
5	*Open*	Enables User and Administrator passwords.	*Open*
	Closed	Clears User and Administrator passwords.	
6	*Open*	CMOS memory acts as a non-volatile store for the Setup program..	*Open*
	Closed	Clears the Setup configuration data in the CMOS memory.	
7		Selects system board speed settings, refer to "Bus Frequencies" on page 72.	
8	*Open*	Disables secure mode.	*Open*
	Closed	Sets the security mode. Sets the switch to the closed position to prevent the BIOS from being upgraded and to disable writing to disks.	
9	*Open*	Disables space-bar power-on. This setting overrides the setting in the Setup program.	*Open*
	Closed	Enables space-bar power-on. If you want to enable this feature, set this switch to Closed. This setting overrides the setting in the Setup program.	
10		Not used.	

Processor Socket

The microprocessor is packaged in a pin-grid-array (PGA), which is seated on the system board in a Zero-Insertion-Force (ZIF) socket.

VRM Socket

P54CS (133 150 and 200 MHz) Pentium processors require a 3.3V supply. Since the PC has a regulated 3.3 V output, a shorting block is used to connect the output directly to the processor.

The P54C 166 MHz Pentium processor requires slightly more than 3.3 V and therefore needs an active VRE voltage regulator module (VRM), in which the voltage is derived from both the 3.3 V and 5 V outlets of the power supply.

Main Memory Sockets

There are six main memory module sockets, arranged in three banks (A to C), allowing installation of up to 128 MB DRAM.

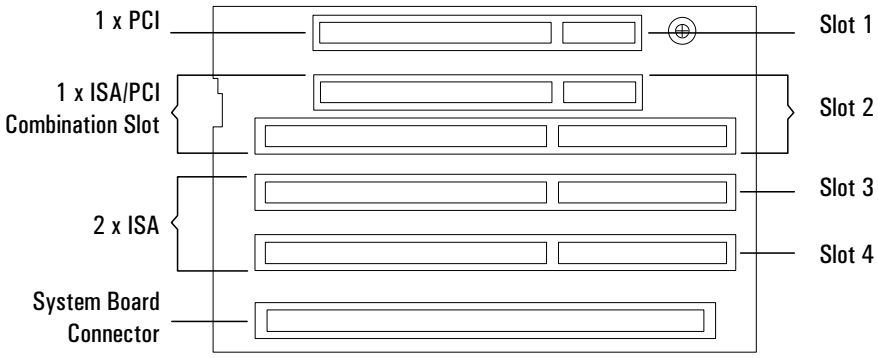
Advanced Power Management (APM)

The Advanced Power Management (APM) is a standard, defined by Intel and Microsoft, for a power-saving mode that is applicable under a wide range of operating systems. The version APM 1.1 supports the following modes: *Fully-on, Standby, Suspend,* and *Off*.

The *Suspend* mode, which also used to be known as *Sleep*, is now managed at the operating system level only. There is no longer the inter-activity between BIOS *Setup* and operating systems, and no longer a “sleep at” item in the *Setup* menus. This is to avoid the BIOS from shutting down the system at the wrong moment.

HP Vectra 500 Series Desktop Backplane

The HP Vectra 500 Series desktop backplane supports two 16-bit ISA (Industry Standard Architecture) cards, one 32-bit PCI (Peripheral Component Interconnect) card and has one combination slot for an ISA or PCI card.

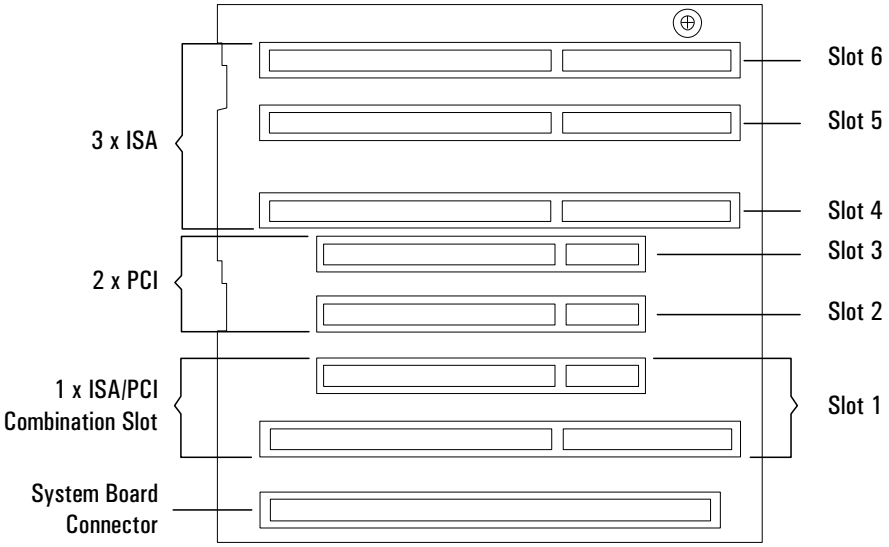


The four expansion card slots are arranged as follows:

- Slot 1 - (the top slot) can be used for a 32-bit PCI card.
- Slot 2 - a combination slot that can be used for a 32-bit PCI card or a full-length 16-bit ISA card (up to 30 cm / 12 inches).
- Slot 3 - can be used for a full-length 16-bit ISA card.
- Slot 4 - can be used for a half-length 16-bit ISA card (up to 15 cm / 6 inches).

HP Vectra 500 Series Minitower Backplane

The HP Vectra 500 Series minitower backplane supports three 16-bit ISA (Industry Standard Architecture) cards, two 32-bit PCI (Peripheral Component Interconnect) cards and has one combination slot for an ISA or PCI card.



The six expansion card slots are arranged as follows:

- Slot 1 - (the innermost) a combination slot that can be used for a half-length 16-bit ISA card (up to 15 cm / 6 inches) or a 32-bit PCI card .
- Slot 2 - can be used for a 32-bit PCI card.
- Slot 3 - can be used for a 32-bit PCI card.
- Slot 4 - can be used for a full length 16-bit ISA card (up to 30 cm / 12 inches).
- Slot 5 - can be used for a full length 16-bit ISA card.
- Slot 6 - can be used for a full length 16-bit ISA card.

Devices on the Processor Local Bus

The following subsystems are associated with the Processor Local bus:

- Intel Pentium microprocessor
- cache memory
- main memory

Pentium Processor

The Pentium processor uses a 64-bit bus, and is 100% compatible with Intel's family of x86 processors. All application software that has been written for Intel 80386 and Intel 80486 processors can run on the Pentium without modification. The Pentium processor contains all the features of the Intel 80486 processor, with the following added features which enhance performance:

- Superscalar Architecture
- Floating Point Unit
- Dynamic Branch Prediction
- Instruction and Data cache
- Data Integrity
- Ability to support MultiProcessor Specification (MPS) 1.1
- PCI bus architecture
- Advanced Power Management capability for reducing power consumption

The processor is seated in a Zero Insertion Force (ZIF) socket.

Superscalar Architecture

The Pentium processor's superscalar architecture has two instruction pipelines and a floating-point unit, each capable of independent operation. The two pipelines allow the Pentium to execute two integer instructions in parallel, in a single clock cycle. This is called instruction pairing. Each instruction must be simple. One pipeline will always receive the next sequential instruction of the one issued to the other pipeline.

Using the pipelines halves the instruction execution time and almost doubles the performance of the processor, compared with an Intel486 microprocessor of the same frequency.

Floating Point Unit (FPU)

The Floating Point Unit incorporates optimized algorithms and dedicated hardware for multiply, divide, and add functions. This increases the processing speed of common operations by a factor of three.

Dynamic Branch Prediction

The Pentium processor uses dynamic branch prediction. To dynamically predict instruction branches, the processor uses two prefetch buffers. One buffer is used to prefetch instruction code in a linear way, and the other to prefetch instruction code depending on the contents of the Branch Target Buffer (BTB). The BTB is a small cache which keeps a record of the last instruction and address used. It uses this information to predict the way that the instruction will branch the next time it is used. When it has made a correct prediction, the branch is executed without delay, thereby enhancing performance.

Instruction and Data Cache

The Pentium processor has separate on-chip code and data caches. Each cache is 8 KB in size with a 32-bit line. The cache acts as temporary storage for data and instructions from the main memory. As the system is likely to use the same data several times, it is faster to get it from the on-chip cache than from the main memory.

Each cache has a dedicated Translation Lookaside Buffer (TLB). The TLB is a cache of the most recently accessed memory pages. The data cache is configured to be Write-Back on a line-by-line basis (a line is an area of memory of a fixed size).

The data cache tags (directory entries used to reference cached memory pages) are triple-ported to support two data transfers and an inquire cycle in the same clock cycle. The code cache tags are also triple-ported to support snooping (a way of tracking accesses to main memory by other devices) and split line accesses.

Individual pages of memory can be configured as cacheable or non-cacheable by software or hardware. They can also be enabled and disabled by hardware or software.

Data Integrity

The processor uses a number of techniques to maintain data integrity. It employs two methods of error detection:

- Data Parity Checking

  This is supported on a byte-by-byte basis, generating parity bits for data addresses sent out of the microprocessor. These parity bits are not used by the external subsystems.

- Internally

  The processor uses functional redundancy checking to provide maximum error detection of the processor and its interface.

Bus Frequencies

The Pentium processor uses internal clock multiplication. For example, a 150 MHz processor multiplies the 60 MHz system clock by 2.5.

Switches 1 and 2 set the frequency of the Processor-Local bus.
Switches 3 and 4 set the clock multiplier ratio (system clock : local bus).
Switch 7 sets the ISA bus speed.

If a processor upgrade is installed, the switch settings may need to be changed to adapt to the new processor. The following table shows the settings required for the different processors.

Switch			**Switch**				
1	**2**	**Processor-Local Bus Frequency**	**3**	**4**	**7**	**Frequency Ratio (Processor: Local Bus)**	**Processor Frequency**
Open	Closed	66 MHz	Open	Open	Closed	1.5	100 MHz
Closed	Open	60 MHz	Closed	Open	Closed	2	120 MHz
Open	Closed	66 MHz	Closed	Open	Closed	2	133 MHz
Closed	Open	60 MHz	Closed	Closed	Closed	2.5	150 MHz

Switch			Switch				
1	2	Processor-Local Bus Frequency	3	4	7	Frequency Ratio (Processor: Local Bus)	Processor Frequency
Open	Closed	66 MHz	Closed	Closed	Closed	2.5	166 MHz
Closed	Open	60 MHz	Open	Closed	Closed	3.0	180 MHz
Open	Closed	66 MHz	Open	Closed	Closed	3.0	200 MHz

The computer will execute erratically, if at all, if the configuration switches are set to operate at a higher processor speed than the processor is capable of supporting. This may cause damage to the PC.

Setting the switches to operate at a slower speed than the processor is capable of supporting would not cause any failure of operation but would cause instructions to be executed more slowly than they should be.

Cache Memory

The PC allows for the provision of two levels of cache memory:

- Level-one cache memory which is fabricated by Intel in the Pentium processor chip
- Level-two cache memory is optionally installed as a memory module on the system board

Each acts as temporary storage for data and instructions from the main memory. Since the system is likely to use the same data several times, it is faster to get it from the on-chip level-one cache than from the main memory.

The level-two cache memory, when fitted, has a 32-byte line size (a line is an area of memory of a fixed size). It is controlled by the PL/PCI bridge chip (SB82437FX). A single HP cache memory module consists of 256 KB of direct mapped, synchronous or asynchronous, static random access memory (SRAM). The synchronous cache memory module achieves 10% better performance than the asynchronous module.

Main Memory

There are six main memory module sockets on the system board, enabling up to 128 MB of main memory to be installed. The sockets are arranged in three banks (A to C). Memory modules must be installed in pairs which are the same size to ensure that all the memory is configured correctly.

Fast memory access, with the timing pattern 7-2-2-2, is achieved by installing EDO RAM. The PC supports 60 ns EDO or 70 ns FPM DRAM.

The PL/PCI bridge chip (SB82437FX-66) provides the dedicated DRAM memory address and data buses. It implements a page mode of operation, allowing one or two pages to be open simultaneously.

The two data path unit chips (SB82438FX), controlled by the PL/PCI bridge chip, implement a 64-bit data path (not interleaved) between the processor local bus and main memory modules. They also provide a buffer, four 64-bit words in depth, which can be used for writes from processor to main memory, level-2 cache write-back cycles, and transfers from PCI to main memory. It also provides a one-level posted write buffer for all processor writes to the PCI bus memory.

Devices on the PCI Bus

The PL/PCI bridge is implemented within the Intel SB82437FX-66 chip (see page 63). It is responsible for transferring data between the Processor-Local bus and the PCI bus.

As a PCI bus slave, this chip becomes the PL bus master, to generate DRAM requests on behalf of other PCI bus masters. It supports PCI bus burst cycles, posted writes to DRAM for PCI burst writes, and read-ahead from DRAM for PCI burst reads.

As a PCI bus master, this chip provides for programmable PCI bus memory regions in the memory address map, and supports PCI bus burst cycles for 64-bit and 32-bit misaligned Pentium reads and writes. It provides optional posting of PCI memory and I/O writes, optional buffering of PCI memory writes, and optional read-ahead for processor to PCI accesses.

As the PCI bus arbiter, it can handle up to four masters, using a rotating priority scheme.

The PCI bus handles the following peripheral devices:

- video controller
- IDE controller
- other devices in the PCI accessory slots.

Video Controller

Depending on the model, the PC uses one of the following:

- An integrated 32/64-bit Ultra VGA controller on the PCI bus, with 1 MB of video memory. Memory can be increased to 2 MB by installing two 512 KB modules.
- A Matrox MGA Millennium card with 2 MB of video memory that can be increased to 4 MB or 8 MB. The Matrox MGA Millennium video card is installed in one of the PCI slots on the backplane. For a full description of the Matrox MGA Millennium video card, refer to “Matrox MGA Millennium Video Controller Card” on page 127.

S3 Trio 64PnP Video Controller

The integrated video subsystem consists of a PCI bus video controller and a DRAM array. The PC uses the S3 Trio 64 PnP video controller. This video controller embeds a RAMDAC, and supports video resolutions of up to 1280 x 1024. The S3 Trio 64PnP video controller offers full compatibility with VGA. In addition, the features are enhanced beyond Super VGA by hardware which accelerates graphical user interface operation in Windows 95.

The enhanced features include:

- Direct connectivity to PCI bus.
- True acceleration for 8, 16 and 32-bit pixel depths.
- 57 MHz clock for video memory.
- Fully programmable Pixel Clock Generator up to 135 MHz.
- Availability to support 2 MB DRAM.
- Fast linear addressing with full software relocation.

Video DRAM

The HP Vectra 500 Series PC is supplied with 1 MB of video DRAM. An additional 1 MB of video DRAM can be installed. The upgrade consists of two 512 KB video memory chips.

Video Resolutions Supported

For a full list of the different video resolutions available, refer to “S3 Trio 64 Video Modes” on page 121, for a table containing all the supported video resolutions.

Integrated Drive Electronics (IDE) Controller

The IDE controller is implemented as part of the PCI/ISA bridge chip (see page 65). It supports Enhanced IDE (EIDE) and Standard IDE (Bus Master IDE). To use the Enhanced IDE features, however, hard disk drives must be compliant with Enhanced IDE.

Up to four IDE devices can be supported: two connected to the primary channel cable, and two to the secondary channel cable. For minitower models, the primary and secondary channels are both fitted with IDE cables

with two connectors. For desktop models, the primary channel cable is fitted with two connectors, and the secondary channel cable is fitted with one connector.

With EIDE, it is possible to have a fast device, such as a hard disk drive, and a slow device, such as a CD-ROM drive, on the same channel without affecting the performance of the fast device. However, in general, the primary channel cable is recommended for hard disk drives, and the secondary channel cable for CD-ROM drives. Indeed, if a CD-ROM is placed on the same channel as a hard disk drive, problems could be experienced activating the 32-bit access drivers.

Other PCI Accessory Devices

PCI expansion cards (accessory boards) are used for high-speed peripheral accessories. Up to three PCI cards can be installed in minitower models, and up to two PCI cards can be installed in desktop models.

Devices on the ISA Bus

ThePCI/ISA Bridge chip (also known as PIIX, or as the system I/O chip, SIO-A) is an Intel SB82371FB. It is responsible for transferring data between the PCI bus and the ISA expansion bus.

As the ISA bus controller, the chip supports asynchronous ISA bus operation up to 16 MHz. It integrates: two DMA controllers, two interrupt controllers, a timer, a hidden ISA refresh controller, support for the BIOS, data buffers to isolate the PCI and ISA buses, and NMI control logic. It also contains the two-channel PCI IDE controller (which is described on page 76).

The ISA bus handles the following devices:

- Super I/O controller.
- Serial EEPROM.
- System ROM.
- Other ISA accessory devices.

Super I/O Chip (SMC FDC37C932)

The basic input/output control functions are provided by the Super I/O chip, the SMC FDC37C932. This chip is 100% compatible with ISA architecture and contains the following:

- Serial / parallel communications ports.
- Flexible drive controller (FDC).
- Keyboard and mouse controller.
- Real time clock (RTC) and CMOS memory.

Serial/Parallel Communications Ports

The Super I/O chip supports two serial ports and one bidirectional parallel port. The serial ports are high-speed UARTs with 16-Byte FIFOs, and can be programmed as COM1, COM2, COM3, COM4, or disabled.

The parallel port can operate in four modes:

- Standard mode (PC/XT, PC/AT, and PS/2 compatible)

- Bidirectional mode (PC/XT, PC/AT, and PS/2 compatible)
- Enhanced mode (Enhanced Parallel Port or EPP compatible)
- High speed mode (MS/HP Extended Capabilities Port or ECP compatible).

  It can be programmed as LPT1 (378h, IRQ7), LPT2 (278h, IRQ5), or disabled.

Floppy Drive Controller (FDC)

The integrated Floppy Drive Controller (FDC) supports 3.5-inch and 5.25-inch floppy disk drives, and tape drives. It is software and register compatible with the 82077AA, and 100% IBM compatible. It has an A and B drive-swapping capability and a non-burst DMA option.

Keyboard and Mouse Controller

The PC has an 8042-based keyboard and mouse controller (the socket pin layouts are as shown on page 24). The C3758A keyboard is supplied for use with the Windows 95 operating system (though it will also work with other operating systems). It has the following capabilities:

- Space-bar power-on, to start the computer from the *Off* state (if **`power on from keyboard`** is enabled in the *Setup* program).
- Windows key (next to the Alt keys), which has the same effect as clicking the Start button on the Windows 95 task bar.
- Pull-down key (next to the right Ctrl key), which has the same effect as clicking the right mouse button.

Real-Time Clock (RTC)

The real-time clock (RTC) is 146818A-compatible. The configuration RAM is implemented as 256 bytes of CMOS memory.

Serial EEPROM

This is non-volatile memory which holds the default values for the CMOS memory (in the event of battery failure, or the user pressing F9 in *Setup*).

System ROM

The PC uses 128 KB of 200 ns, Flash EEPROM implemented within a single 256 K X 8-bit ROM chip. This is a ROM that can be returned to its unprogrammed state, by the application of appropriate electrical signals to its pins, and then reprogrammed with the latest upgrade firmware.

The System ROM contains the system BIOS (including the boot code, the ISA and PCI initialization, RPO, DMI, the Setup program and the Power-On Self-Test routines, plus their error messages).

Refer to chapter 4, Summary of the HP/Phoenix BIOS, for more information on the BIOS.

Other ISA Accessory Devices

ISA expansion cards (accessory boards) are for slow peripheral accessories. For minitower models, there are four slots on the ISA bus for expansion cards (although one of these is a combination slot with the PCI bus). For desktop models, there are three slots on the ISA bus for expansion cards (although one of these is a combination slot with the PCI bus).

4

Summary of the HP/Phoenix BIOS

This chapter gives an overview of the two different versions of the HP/Phoenix BIOS installed on the HP Vectra 500 Series PC models.

Overview

The information concerning the different versions of the HP/Phoenix BIOS installed on the HP Vectra 500 Series models described in this chapter is divided into two main sections:

- The system BIOS identified by the version number **GX.07.xx**, installed on the HP Vectra 500 Series PC models with an HP Service Part Number: D4051-63001. For a complete list of the computers associated with this part number, refer to “D4051-63001 Models” on page 15.
- The system BIOS identified by the version number **GJ.07.xx** installed on the HP Vectra 500 Series PC models with the HP Service Part Numbers: D3657-63001 and D3661-63001. For a complete list of the computers associated with these part numbers, refer to “D3657-63001 Models” on page 16 and “D3661-63001 Model” on page 17.

HP/Phoenix BIOS Description

The System ROM contains the system BIOS (including the boot code, the ISA and PCI initialization, DMI, the *Setup* program and the Power-On Self-Test routines, plus their error messages).

The PC uses 128 KB of 200ns, Flash EEPROM implemented within a single 256 K × 8-bit ROM chip. This is a ROM that can be returned to its unprogrammed state, by the application of appropriate electrical signals to its pins, and then reprogrammed with the latest upgrade firmware.

Updating the System ROM

The System ROM can be updated with the latest BIOS firmware. It can be ordered from HP or downloaded from one of the HP online services.

The System ROM is updated by running the PHLASH utility, **`PHLASH.EXE`**, which is supplied with the BIOS upgrade file, **`NN07xx.FUL`**, and the system definition file, **`platform.bin`**. You must specify the *model number* of the PC since the utility which is supplied for a different model cannot be used with this one. It must be run from a diskette.

Before flashing, it is necessary to disable the “Secure Mode” switch on the system switches, and to type in the System Administrator Password when starting up the computer. The PCI and PnP information is erased in the process.

Do not switch off the computer until the system BIOS update procedure has completed, successfully or not, since irrecoverable damage to the ROM may otherwise be caused. While updating the flash ROM, the power supply switch and the reset button are disabled to prevent accidental interruption of the flash programming process.

When installing a new system board, the ROM will have a blank serial number field. This will be detected automatically by the BIOS. Depending on the type of system board, you may or may not be prompted to enter the serial number. The serial number is printed on the identification label on the back of the PC.

Error Diagnostics and Suggested Corrective Actions

The programs and data in the system ROM are accompanied by a check-sum code. If any of the programs or data ever become corrupted, the check-sum will not correspond with the contents of the ROM, and the appropriate part of the POST routine will attempt to report the error:

```
Cannot display error messages
Flash ROM may be defective
```

The suggested corrective action is to reprogram the system ROM by running the same utility as is normally used for upgrading it.

Little Ben

Little Ben is an HP application specific integrated circuit (ASIC) that is connected between the chipset and the processor. It has been designed to act as a companion to the Super I/O chip. It contains the following:

- Hard and soft power control.
- BIOS timer:
  hardware-wired, 50 ms long 80 Hz beep module;
  automatic blinker that feeds the LEDs module with a 1 Hz oscillator signal.
- Flash access and protection (supporting 128, 256 or 512 ROMs).
- Super I/O protection.
- Glue logic:
  Support for SMIs (for Intel's SMM mode). Enhanced keyboard lock and external wake-up;
  IRQ generator controlled by software;
  SMI generator controlled by software;
  Programmable chip selects.
- 16-bit address decoding and remapping.
- Four general purpose I/O (Input/Output).

Little Ben is powered by battery, so its consumption has to be as low as possible. When *VccState* and *PowerGood* pins are both low, all output pins are in tri-state mode, except for *RemoteOnBen* which continues to be driven. This allows the PC to be restarted even after a power loss has occurred.

If the BIOS needs to turn off the PC, it must ensure that the PC is not locked by Little Ben's lock bit. If it is, the power remains on, a red light is illuminated, and a buzzer is activated.

HP/Phoenix BIOS (BIOS version: GX.07.xx)

This section gives an overview of the HP/Phoenix BIOS identified by the BIOS version: GX.07.xx associated with the HP Vectra 500 Series models, HP Service Part Number D4051-63001.

The information in this section includes the following:

- *Setup* Program: with menu-driven context-sensitive help (in U.S. English only).
- I/O Addresses Used by the System: the address space, with details of the interrupts used, described in the section I/O Addresses Used by the System (BIOS version: GX.07.xx), on page 90.
- The Power-On Self-Test or POST, which is the sequence of tests the PC performs to ensure that the system is functioning correctly, described in the section Power-On Self-Test (BIOS version: GX.07.xx), on page 94.

Setup Program (BIOS version: GX.07.xx)

You can interrupt the POST to run the *Setup* program by pressing F2 when the **F2=Setup** message appears on the initial "Vectra" logo screen.

The band along the top of the screen offers five menus: Main, Configuration, Security, Power, and Exit. To select one of these, simply move to the appropriate name, using the left and right arrow keys. Each menu is discussed below.

Main Menu (BIOS version: GX.07.xx)

The Main Menu presents the user with a list of fields, such as "System Time" and "Key click". These can be selected using the up and down arrow keys, and can have their values changed using the F7 and F8 keys.

The "Item-Specific Help" field changes automatically as the user moves the cursor between the fields. It tells the user what the currently highlighted field is for, and what the options are.

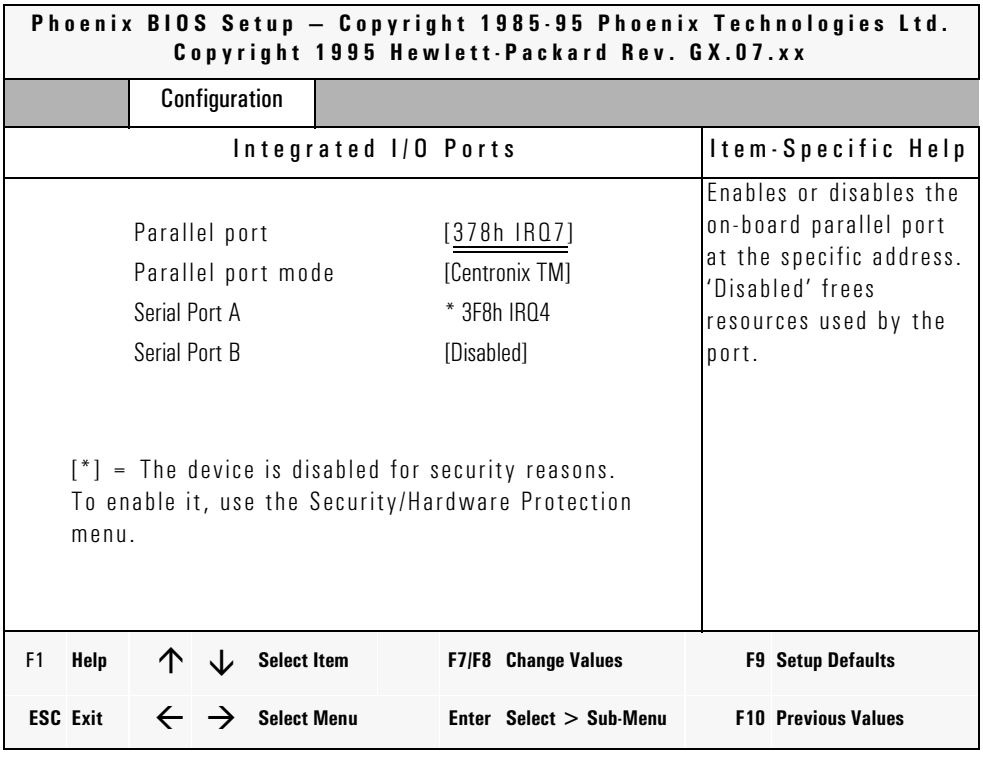
Some fields are not changeable. Examples include fields that are for information only, and fields whose contents become "frozen" by the setting of a value in some other field. Such fields are displayed in a different color, without the "[" and "]" brackets. When the user moves the cursor with the up and down arrow keys, such fields are skipped.

Some fields disappear completely when a choice in another field makes their appearance inappropriate (for example, the “Key auto-repeat speed” and “Delay before auto-repeat” fields disappear when the user selects **Yes** in the “Running Windows 95” field, since these parameters can then be set within the operating system).

Configuration Menu (BIOS version: GX.07.xx)

The Configuration Menu does not have the same structure as the Main Menu and Power Menu. Instead of presenting a list of fields, it offers the user a list of sub-menus. Again, the user steps between the options using the up and down arrow keys, but presses the Enter key to enter the chosen sub-menu (and the Esc key to go back again when finished).

If access to devices has been disabled in the Security Menu, then the configuration of those devices on the Configuration Menu becomes frozen, as shown in the diagram below for Serial port A. The field becomes starred, appears in a different color and cannot be changed.



Disabling a device in the Configuration Menu (for example, Serial port B in the diagram above) has the advantage of freeing the resources (such as IRQs and peripheral addresses). Disabling a device in the Security Menu disables the access, does not free the resources, but has the advantage of temporarily disabling the device without losing the configuration settings.

Under the "Memory and Cache" sub-menu, memory caching can be set to **`internal only`**, **`disabled`** or **`both`**; the memory hole can be **`enabled`** between 15 MB and 16 MB[1]; the graphic POST can be **`disabled`** if there is a Display Option ROM installed; the shadow/cache ISA option ROMs can be made accessible if detected as being fitted.

Under the "IDE" sub-menu, multi-sector transfers can be **`disabled`**, or set to **`2`**, **`4`**, **`8`**, or **`16`**; the translation method can be set to **`extended`** or **`standard`**; the integrated bus adapters can be set to **`none`**, **`primary=IRQ15`**, **`secondary=IRQ14`**, or **`both`**.

Security Menu (BIOS version: GX.07.xx)

Sub-menus are presented for changing the characteristics and values of the User Password, the System Administrator Password, the amount of protection against use of the system's drives and network connections (using the Hardware Protection sub-menu), and the amount of protection against being able to boot from the system's drives and network connections (using the Start-Up Centre sub-menu).

The minimum lengths of either type of password can be set to a specific number of characters, or to **`none`**. The maximum length of each is 32 characters. A limit can be set for the maximum number of retries that are permitted if the password is mistyped, and whether a delay should be imposed (of successively increasing lengths: 4 seconds, 8 seconds, 16 seconds, and finally 32 seconds) before successive retries are accepted (using the **`exponential`** setting for the "Lock Time Between Attempts" field).

The "User Password" sub-menu grants access to the keyboard lock timer option. Once this password has been set, the menu gives access to the main sub-menu of user preferences.

Under the "Hardware Protection" sub-menu, the following devices can have their access **`unlocked/locked`**: flexible disk controller, IDE controllers, serial and parallel ports, network controller. Writes to the flexible disk can

1. available only if ≥ 16 MB.

be **locked**, so as to prevent the exporting of data. Writes to the hard disk drive boot sector can also be **locked**, for instance as a protection against viruses.

Under the "Start-Up Center" sub-menu, the *Setup* program not only allows the user to select which devices are to be used (**yes** or **no**) for booting up the system, but also indicates their order of precedence when more than one is enabled: flexible disk drive, CD-ROM drive, or hard disk drive.

Power Menu (BIOS version: GX.07.xx)

The "Power" menu allows the user to set the standby delay. It also allows the system administrator to decide whether the mouse is enabled as a means of reactivating the system from *Standby*. It is also possible to specify whether the space-bar is enabled as a means of reactivating the system from *Off*.

Summary Configuration Screen (BIOS version: GX.07.xx)

You can press F2 while the initial "Vectra" logo screen is being displayed to run the *Setup* program (as described in the previous sub-sections). Alternatively, you can press Esc to view the summary configuration screen, an example of which is depicted on the next page. By default, this remains on the screen for 20 seconds, but by pressing F5 once, it can be held on the screen until F5 is pressed again, or until F1 is pressed. Pressing F10 will cause the PC to be turned off.

The following summary screen is an example of a system configuration.

HP Vectra VE5/100 Series 3 – Copyright 1995 Hewlett-Packard – QA.01.00			
Any line of text can be entered here as a 'tatoo' for the PC			
BIOS Version	: GX.07.xx	PC Serial Number	: 0000A00000
CPU Date Code	: N/A		
System RAM	: 15 MB	COM1	: 3F8H (Serial A)
Bank A	: 8 MB (EDO)	COM2	: 2F8H (Serial B)
Bank B	: 8MB (EDO)	COM3	: 3E8H (external)
Bank C	: None	COM4	: None
Video RAM	: 1 MB	LPT1	: 378H
System Cache	: 256 KB (synchronous)	LPT2	: None
Video Device	: SiS	LPT3	: None
1st IDE Device	: HDD 1279 MB	Flexible Disk A	: 1.44 MB
2nd IDE Device	: None	Flexible Disk B	: None
3rd IDE Device	: None	Display type	: Not Available
4th IDE Device	: None		
ISA PnP	: AZT3001 PnP Sound Device	PCI Slot	: Not Installed
ISA PnP	: Not Installed	PCI Slot	: Not Installed
ISA PnP	: Not Installed	PCI Slot	: Not Installed
ISA PnP	: Not Installed		
<F1> to continue, <F2> to run SETUP, <F10> to power off, <F5> to retain			

I/O Addresses Used by the System (BIOS version: GX.07.xx)

Peripheral devices, accessory devices and system controllers are accessed via the system I/O space. The 64 KB of addressable I/O space comprises 8-bit and 16-bit I/O ports (these are registers that are located in the various system components). When installing an expansion card, ensure that the I/O address space selected is in the free area of the space reserved for expansion cards (100h to 3FFh).

100h-109h	HP reserved
15Ch-15Dh	I/O controller
170h-177h, 376h	IDE controller secondary channel
1F0h-1F7h, 3F6h	IDE controller primary channel
278h-27Fh, 378h-37Fh	Parallel port
2E8h-2EFh, 2F8h-2FFh, 3E8h-3EFh, 3F8h-3FFh	Serial port
370h-371h	Integrated I/O Controller
3B0h-3DFh	Integrated video graphics controller
3F0h-3F5h, 3F7h	Integrated floppy disk drive controller
496h-497h	HP reserved
678h-67Bh	Parallel port if ECP mode is selected
778h-77Bh	Parallel port if ECP mode is selected

Refer to the BIOS I/O Port Map (BIOS version: GX.07.xx), on page 91 for more detailed information.

System Memory Map (BIOS version: GX.07.xx)

00000h - 9FFFFh	640 KB–Base Memory Area
A0000h - BFFFFh	128 KB–Video Memory
C0000h - C7FFFh	32 KB–Video BIOS
C8000h - DFFFFh	96 KB–Expansion Cards Memory
E0000h - EFFFFh	64 KB–Available
F0000h - FFFFFh	64 KB–System BIOS
100000h - FFFFFFFFh	1 MB plus–Extended Memory

Reserved memory used by expansion cards must be located in the area from C8000h to EFFFFh.

BIOS I/O Port Map (BIOS version: GX.07.xx)

This section describes the HP BIOS port map. The next section provides more details about how the BIOS uses the system board components mentioned in the I/O port list.

I/O Address Ports	Function	Bits
0000-000F	DMA controller 1	8
0020-0021	Interrupt controller 1	8
0040-0043	Interval timer 1	8
0060, 0064	Keyboard controller	8
0061	NMI status and control	8
0070	NMI mask register, RTC address	8
0071	RTC data	8
0081-0083, 008F	DMA low page register	8
0092	Alternate reset and A20 Function	8
00A0-00A1	Interrupt controller 2	8
00C0-00DF	DMA controller 2	8
00F0-00FF	Co-processor error	
0100-0109	HP reserved	
015C-015D	I/O Controller	
0170-0177	IDE controller secondary channel	
01F0-01F7	IDE controller primary channel	
0278-027F	Parallel port 3	
02E8-02EF	Serial Port 4	
02F8-02FF	Serial Port 2	
0370-0375	Secondary floppy disk controller	
0376	IDE controller secondary channel	
0377	Secondary floppy disk controller	

I/O Address Ports	Function	Bits
0378-037F	Parallel port 2	
03B0-03BB	Integrated video graphics controller	
03BC--03BF	Parallel port 1	
03C0-03DF	Integrated video graphics controller	
03E8-03EF	Serial port 3	
03F0-03F5	Floppy disk controller	
03F6	IDE controller primary channel	
03F7	Floppy disk controller	
03F8-03FF	Serial port 1	
0496-0497	Internal ports (or HP reserved)	
0CF8-0CFF	Used for PCI configuration[1]	

[1] These addresses are dedicated to configuration registers for PCI devices.

System Board Components (BIOS version: GX.07.xx)

This section provides more details of how the BIOS uses the system board components mentioned in the I/O port list.

DMA Channel Controllers (BIOS version: GX.07.xx)

Only “I/O-to-memory” and “memory-to-I/O” transfers are allowed. “I/O-to-I/O” and “memory-to-memory” transfers are disallowed by the hardware configuration.

The system controller supports seven DMA channels, each with a page register used to extend the addressing range of the channel to 16 MB.

The following table summarizes how the DMA channels are allocated.

First DMA controller (used for 8-bit transfers)	
Channel	**Function**
0	Available
1	Available or ECP mode for parallel port
2	Flexible disk I/O
3	Available or ECP mode for parallel port
Second DMA controller (used for 16-bit transfers)	
Channel	**Function**
4	Cascade from first DMA controller
5-6	Available
6-7	Available

Interrupt Controllers

(BIOS version: GX.07.xx)

The system has two 8259A compatible interrupt controllers. They are arranged as a master interrupt controller and a slave that is cascaded through the master.

The following table shows how the master and slave controllers are connected. As the HP Vectra 500 Series incorporates the Plug and Play mode, some of the IRQ settings indicated in the following table could be different. This table should be used as a guideline only. The Interrupt Requests (IRQ) are numbered sequentially, starting with the master controller, and followed by the slave.

IRQ (Interrupt Vector)		Interrupt Request Description
IRQ0(08h)		System timer
IRQ1(09h)		Keyboard controller
IRQ2(0Ah)	Slave IRQ	Cascade connection from INTC2 (Interrupt Controller 2)
	IRQ8(70h)	Real time clock
	IRQ9(71h)	Available for PCI expansion cards, if not used by ISA boards
	IRQ10(72h)	Available for PCI expansion cards, if not used by ISA boards
	IRQ11(73h)	Available for PCI expansion cards, if not used by ISA boards
	IRQ12(74h)	Mouse
	IRQ13(75h)	Pentium
	IRQ14(76h)	Primary channel of IDE controller

	IRQ15(77h)	Free, if not used by secondary channel of IDE controller
IRQ3(0Bh)		Free, if not used for serial port
IRQ4(0Ch)		Free, if not used for serial port
IRQ5(0Dh)		Free, if not used for parallel port
IRQ6(0Eh)		Floppy disk drive controller
IRQ7(0Fh)		Free, if not used for parallel port

Using the *Setup* program:

- IRQ3 can be made available by disabling serial ports 2 and 4.
- IRQ4 can be made available by disabling serial ports 1 and 3.
- IRQ5 can be made available by disabling the parallel port 2.
- IRQ7 can be made available by disabling parallel ports 1 and 2.
- IRQ12 can be made available by disabling the mouse interrupt.

PCI Interrupt Request Lines (BIOS version: GX.07.xx)

PCI devices generate interrupt requests using up to four PCI interrupt request lines (INTA#, INTB#, INTC#, and INTD#).

When a PCI device makes an interrupt request, the request is re-directed to the system interrupt controller. The interrupt request will be re-directed to one of the IRQ lines made available for PCI devices.

All PCI devices with interrupt transfer support will use and share INTA#. A multiple-function PCI device may use several INT lines. These devices will require more than one system interrupt request line.

Power-On Self-Test (BIOS version: GX.07.xx)

This section describes the Power-On Self-Test (POST) routines, which are contained in the PC's ROM BIOS, the error messages which can result, and the suggestions for corrective action.

Each time the system is powered on, or a reset is performed, the POST is executed. The POST process verifies the basic functionality of the system components and initializes certain system parameters. The POST performs the tests in the order described in the table on the next page.

The POST starts by displaying a graphic screen with the initial HP "Vectra" logo. If the POST detects an error, the error message is displayed inside a *view system errors* screen, in which the *error message utility* (EMU) not only displays the error diagnosis, but the suggestions for corrective action. Error codes are no longer displayed.

To see the tests performed during the POST, press Esc when the initial HP "Vectra" logo appears, and the display will switch to text mode. In this mode, a summary configuration screen will be displayed at the end of the POST.

Devices, such as memory and hard disks, are configured automatically. The user is not requested to confirm the change. However, the user is prompted if a device is found to have gone missing since the previous boot. The user can simply accept the new configuration by pressing F4.

During the POST, the BIOS and other ROM data are copied into high-speed shadow RAM. The shadow RAM is addressed at the same physical location as the original ROM in a manner which is completely transparent to applications. It therefore appears to behave as very fast ROM. This technique provides faster access to the system BIOS firmware.

The table on the following page lists the POST routines in the order in which they are executed (from the shadow RAM). If the POST is initiated by a soft reset Ctrl Alt and Delete, the RAM tests are not executed and shadow RAM is not cleared. In all other respects, the POST executes in the same way following power-on or a soft reset.

Test	Description
System BIOS Tests	
LED Test	Tests the LEDs on the control panel.
Processor Test	Tests the processor's registers. Test failure causes the boot process to abort.
System (BIOS) ROM Test	Calculates an 8-bit checksum. Test failure causes the boot process to abort.
RAM Refresh Timer Test	Tests the RAM refresh timer circuitry. Test failure causes the boot process to abort.
Interrupt RAM Test	Checks the first 64 KB of system RAM used to store data corresponding to various system interrupt vector addresses. Test failures cause the boot process to abort.
Shadow the System ROM BIOS	Tests the system ROM BIOS and shadows it. Failure to shadow the ROM BIOS will cause an error code to display. The boot process will continue, but the system will execute from ROM. This test is not performed after a soft reset (using Ctrl Alt and Delete).
Load CMOS Memory	Checks the serial EEPROM and returns an error code if it has been corrupted. Copies the contents of the EEPROM into CMOS RAM.
CMOS RAM Test	Checks the CMOS RAM for start-up power loss, verifies the CMOS RAM checksum(s). Test failure causes error codes to display.

Internal Cache Memory Test	Tests the processor's internal level-one cache RAM. Test failure causes an error code to display and the boot process to abort.
Video Tests	
Initialize the Video	Initializes the video subsystem, tests the video shadow RAM, and, if required, shadows the video BIOS. A failure causes an error code to display, but the boot process continues.
System Board Tests	
Test External Cache	Tests the level-two cache. A failure causes an error code to display and disables the external cache.
Shadow SCSI ROM	Tests for the presence of HP SCSI ROMs. If SCSI ROMs are detected, their contents are copied into the shadow RAM area. A failure will cause an error code to display.
8042 Self-Test	Downloads the 8042 and invokes the 8042 internal self-test. A failure causes an error code to display.
Timer 0/Timer 2 Test	Tests Timer 0 and Timer 2. Test failure causes an error code to display.
DMA Subsystem Test	Checks the DMA controller registers. Test failure causes an error code to display.
Interrupt Controller Test	Tests the Interrupt masks, the master controller interrupt path (by forcing an IRQ0), and the industry-standard slave controller (by forcing an IRQ8). Test failure causes an error code to display.
Real-Time Clock Test	Checks the real-time clock registers and performs a test that ensures that the clock is running. Test failure causes an error code to display.
Memory Tests	
RAM Address Line Independence Test	Verifies the address independence of real-mode RAM (no address lines stuck together). Test failure causes an error code to display.
Size Extended Memory	Sizes and clears the protected mode (extended) memory and writes the value into CMOS bytes 30h and 31h. If the system fails to switch to protected mode, an error code is displayed.
Real-Mode Memory Test (First 640KB)	Read/write test on real-mode RAM. (This test is *not* done during a reset using Ctrl Alt and Delete). The test checks each block of system RAM to determine how much is present. Test failure of a 64 KB block of memory causes an error code to display, and the test is aborted.
Shadow RAM Test	Tests shadow RAM in 64-KB segments (except for segments beginning at A000h, B000h, and F000h). If they are *not* being used, segments C000h, D000h and E000h are tested. Test failure causes an error code to display.
Protected Mode RAM Test (Extended RAM)	Tests protected RAM in 64 KB segments above 1 MB. (This test is *not* done during a reset using Ctrl Alt and Delete). Test failure causes an error code to display.
Keyboard / Mouse Tests	
Keyboard Test	Invokes a built-in keyboard self-test of the keyboard's microprocessor and tests for the presence of a keyboard and for stuck keyboard keys. Test failure causes an error code to display.

Mouse Test	If a mouse is present, invokes a built-in mouse self-test of the mouse's microprocessor and for stuck mouse buttons. Test failure causes an error code to display.
Tests of Flexible Disk Drive A	
Flexible Disk Controller Subsystem Test	Tests for proper operation of the flexible disk controller. Test failure causes an error code to display.
Coprocessor Tests	
Internal Numeric Coprocessor Test	Checks for proper operation of the numeric coprocessor part of the processor. Test failure causes an error code to display.
Parallel Port Tests	
Parallel Port Test	Tests the integrated parallel port registers, as well as any other parallel ports. Test failure causes an error code to display.
Serial Port Tests	
Serial Port Test	Tests the integrated serial port registers, as well as any other serial ports. Test failure causes an error code to display.
Hard Disk Drive Tests	
Hard Disk Controller Subsystem Test	Tests for proper operation of the hard disk controller. Test failure causes an error code to display. The test does not detect hard disk replacement or changes in the size of the hard disk.
System Configuration Tests	
System Generation	Initiation of the system generation (SYSGEN) process, which compares the configuration information stored in the CMOS memory with the actual system. If a discrepancy is found, an error code will be displayed.
Plug and Play Configuration	Configures any Plug and Play device detected (either PCI or ISA): ❒ All PCI devices, and any ISA device necessary for loading the operating system will be configured for use. ❒ Any ISA device that is not required for loading the operating system, will be initialized (prepared for loading of a device driver), but not fully configured for use.

Error Messages (BIOS version: GX.07.xx)

When the PC is switched on or reset, a power-on hardware test is performed. If an error occurs, an error message is displayed.

HP's new-style BIOS does not display POST error codes (such as 910B). These were displayed in the BIOS of previous HP Vectra PCs.

Message	Corrective Action and/or Explanation
Operating system not found	Check whether the disk, HDD, FDD or CD-ROM disk drive is connected. If it is connected, check that it is detected by *Setup.* Check that your boot device is enabled on the *Setup* Security menu. If the problem persists, check that the boot device contains the operating system.
Missing operating system	If you have configured HDD user parameters, check that they are correct. Otherwise, use HDD type "Auto" parameters.
Failure fixed disk (preceded by a 30" time-out)	Check that HDD is connected. Check that HDD is detected in *Setup*. Check that boot on hard disk drive is enabled in *Setup*.
Diskette Drive A (or B) error	Check whether the diskette drive is connected. Check *Setup* for the configuration.
System battery is dead	You may get this message if the PC is disconnected for a few days. When you Power-on the PC, run *Setup* to update the configuration information. The message should no longer be displayed. Should the problem persist, replace the battery.
Keyboard error	Check that the keyboard is connected.
Resource Allocation Conflict -PCI device 0079 on motherboard	Clear CMOS.
Video Plug and Play interrupted or failed Re-enable in Setup and try again	You may have powered your PC Off/On too quickly and the PC turned off Video plug and play as a protection.
System CMOS checksum bad - run Setup	CMOS contents have changed between 2 power-on sessions. Run *Setup* for configuration.
I/O device IRQ conflict	Serial ports A and B may have been assigned the same IRQ. Assign a different IRQ to each serial port and save the configuration.
No message, system "hangs" after POST	Check that cache memory and main memory are correctly set in their sockets.
Other	An error message may be displayed and the PC may "hang" for 20 seconds and then beep. The POST is probably checking for a mass storage device which it cannot find and the PC is in Timeout Mode. After Timeout, run *Setup* to check the configuration.

Beep Codes (BIOS version: GX.07.xx)

If a terminal error occurs during POST, the system issues a beep code before attempting to display the error. Beep codes are useful for identifying the error when the system is unable to display the error message.

Beep Pattern	Numeric Code	Description
-	B4	This does not indicate an error. There is one short beep before system startup.
— --	98	Video configuration failure or Option ROMs checksum failure
— -- -- ---	16H	BIOS ROM checksum failure
— --- — —	20H	DRAM refresh test failure
— --- — ---	22H	8742 Keyboard controller test failure
— --- ----- —	2C	RAM failure
— --- ----- ---	2E	RAM failure on data bits in low byte of memory bus
— ----- — —	30	RAM failure on data bits in high byte of memory bus
-- — -- ---	46	ROM copyright notice check failure
-- -- --- —	58	Unexpected interrupts test failure

HP/Phoenix BIOS (BIOS version: GJ.07.xx)

This section gives an overview of the HP/Phoenix BIOS identified by the version number GJ.07.xx associated with the HP Vectra 500 Series models, HP Service part numbers: D3657-63001 and D3661-63001.

The information in this section is divided into three main sub-sections:

- *Setup* Program: with menu-driven context-sensitive help (in U.S. English only).
- I/O Addresses Used by the System: the address space, with details of the interrupts used, described in the section I/O Addresses Used by the System (BIOS version: GJ.07.xx), on page 104.
- The Power-On-Self-Test or POST, which is the sequence of tests the PC performs to ensure that the system is functioning correctly, described in the section Power-On Self-Test (BIOS version: GJ.07.xx), on page 109.

Setup Program (BIOS version: GJ.07.xx)

You can interrupt the POST to run the *Setup* program by pressing F2 when the **F2=Setup** message appears on the initial "Vectra" logo screen.

The band along the top of the screen offers six menus: Main, Preferences, Configuration, Security, Power, and Exit. To select one of these, simply move to the appropriate name, using the left and right arrow keys. Each menu is discussed below.

Main Menu (BIOS version: GJ.07.xx)

The Main Menu presents the user with a list of fields, such as "System Time" and "Running Windows 95". These can be selected using the up and down arrow keys, and can have their values changed using the F7 and F8 keys.

The "Item-Specific Help" field changes automatically as the user moves the cursor between the fields. It tells the user what the currently highlighted field is for, and what the options are.

Some fields are not changeable. Examples include fields that are for information only, and fields whose contents become "frozen" by the setting of a value in some other field. Such fields are displayed in a different color, without the "[" and "]" brackets. When the user moves the cursor with the up and down arrow keys, such fields are skipped. Some fields disappear completely when a choice in another field makes their appearance inappropriate).

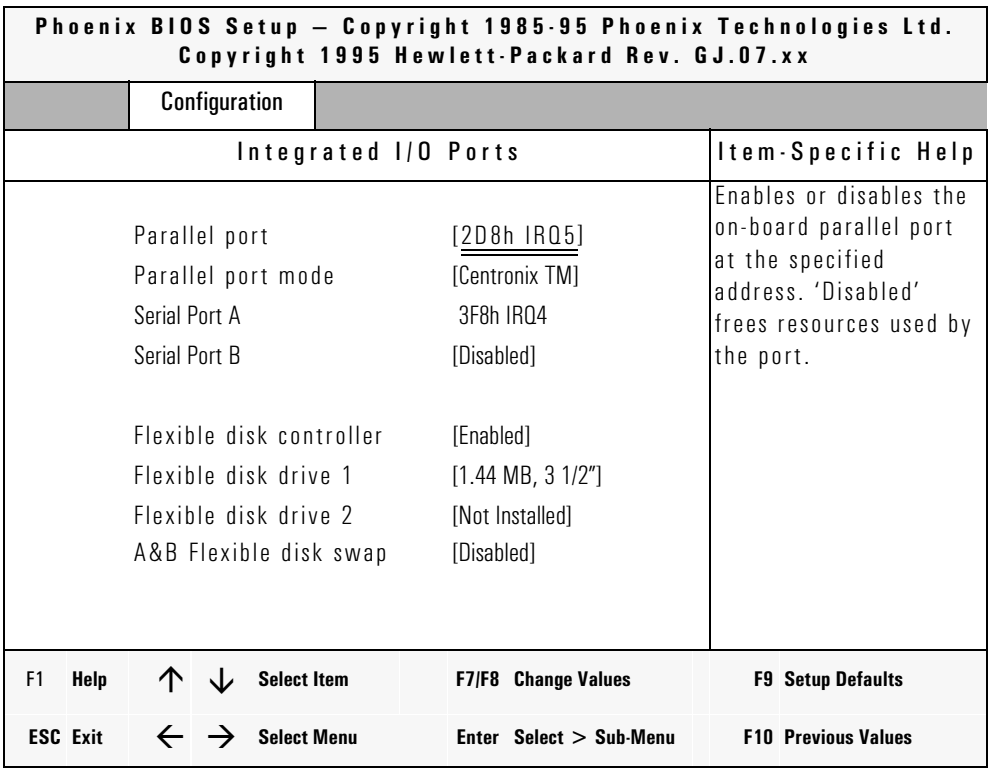
Preferences Menu (BIOS version: GJ.07.xx)

The Preferences Menu has the same menu structure as the Main Menu and Power Menu. This menu allows the user to set a password to prevent unauthorized access to the computer. To set a user password, the administrator password has to be set first.

Configuration Menu (BIOS version: GJ.07.xx)

The Configuration Menu does not have the same structure as the Main Menu, Preferences Menu and Power Menu. Instead of presenting a list of fields, it offers the user a list of sub-menus. Again, the user steps between the options using the up and down arrow keys, but presses the Enter key to enter the chosen sub-menu (and the Esc key to go back again when finished).

If access to devices have been disabled in the Security Menu, then the configuration of those devices on the Configuration Menu becomes frozen.



Disabling a device in the Configuration Menu (for example, Serial port B in the diagram above) has the advantage of freeing the resources (such as IRQs and peripheral addresses). Disabling a device in the Security Menu disables the access, does not free the resources, but has the advantage of temporarily disabling the device without losing the configuration settings.

Under the "Memory and Cache" sub-menu, memory caching can be set to **both, internal only** or **disabled**; the memory hole can be **enabled** between 15 MB and 16 MB; the graphic POST can be **disabled** if there is a Display Option ROM installed; the shadow/cache ISA option ROMs can be made accessible if detected as being fitted.

Under the "IDE" sub-menu, multi-sector transfers can be **disabled**, or set to **2**, **4**, **8**, or **16**; the translation method can be set to **extended** or **standard**; the integrated bus adapters can be set to **none**, **primary only**, **disabled**, or **both**.

Security Menu (BIOS version: GJ.07.xx)

Sub-menus are presented for changing the characteristics and values of the User Password and the System Administrator Password.

The "User Password" sub-menu grants access to the keyboard lock timer option. Once this password has been set, the menu gives access to the main sub-menu of user preferences.

Power Menu (BIOS version: GJ.07.xx)

The "Power" menu allows the user to set the standby delay. It also allows the system administrator to decide whether the mouse is enabled as a means of reactivating the system from *Standby*. It is also possible to specify whether the space-bar is enabled as a means of reactivating the system from *Off*.

Summary Configuration Screen (BIOS version: GJ.07.xx)

You can press F2 while the initial "Vectra" logo screen is being displayed to run the *Setup* program (as described in the previous sub-sections). Alternatively, you can press Esc to view the summary configuration screen. This is displayed for a few seconds only, but it is possible to "freeze" it so the configuration can be checked. Press the Pause/Break key to "freeze" the summary screen.

The following summary screen is an example of a system configuration.

CPU [133 MHz]	: Pentium	System Rom	: F0DC - FFFF
Coprocessor	: Installed	BIOS Version	: GJ.07.17
System RAM	: 640 Kb	COM Ports	: 03F8, 02F8, 03E8
Extended RAM	: 7168 Kb	LPT Ports	: 02D8
Shadow RAM	: 384 Kb	Display Type	: EGA \ VGA
Cache RAM	: None	PS/2 Mouse	: Installed
Hard Disk 0	: 544 Mb	Diskette A	: 1.44 MB
Hard Disk 1	: None	Diskette B	: None
Hard Disk 2	: None	Flexible Disk B	: None
Hard Disk 3	: None		

I/O Addresses Used by the System (BIOS version: GJ.07.xx)

Peripheral devices, accessory devices and system controllers are accessed via the system I/O space. The 64 KB of addressable I/O space comprises 8-bit and 16-bit I/O ports (these are registers that are located in the various system components). When installing an expansion card, ensure that the I/O address space selected is in the free area of the space reserved for expansion cards (100h to 3FFh).

170h-177h, 376h	IDE controller secondary channel
1F0h-1F7h, 3F6h	IDE controller primary channel
278h-27Fh, 378h-37Fh	Parallel port
2E8h-2EFh, 2F8h-2FFh, 3E8h-3EFh, 3F8h-3FFh	Serial port
370h-371h	Integrated I/O Controller
3B0h-3DFh	Integrated video graphics controller
3F0h-3F5h, 3F7h	Integrated floppy disk drive controller
496h-497h	HP reserved
678h-67Bh	Parallel port if ECP mode is selected
778h-77Bh	Parallel port if ECP mode is selected

Refer to the BIOS I/O Port Map (BIOS version: GJ.07.xx), on page 105 for more detailed information.

System Memory Map (BIOS version: GJ.07.xx)

00000h - 9FFFFh	640 KB–Base Memory Area
A0000h - BFFFFh	128 KB–Video Memory
C0000h - C7FFFh	32 KB–Video BIOS
C8000h - DFFFFh	96 KB–Expansion Cards Memory
E000h - EFFFFh	64 KB–Available
F0000h - FFFFFh	64 KB–System BIOS
100000h - FFFFFFFFh	1 MB plus–Extended Memory

NOTE

Reserved memory used by expansion cards must be located in the area from C8000h to EFFFFh.

BIOS I/O Port Map (BIOS version: GJ.07.xx)

This section describes the HP BIOS port map. The next section provides more details about how the BIOS uses the system board components mentioned in the I/O port list.

I/O Address Ports	Function	Bits
0000-000F	DMA Controller 1	8
0020-0021	Interrupt Controller 1	8
0040-0043	Interval Timer 1	8
0060, 0064	Keyboard Controller	8
0061	NMI Status and Control	8
0070	NMI Mask register, RTC address	8
0071	RTC data	8
0081-0083, 008F	DMA Low Page register	8
0092	Alternate reset and A20 Function	8
0096-009F	Internal Ports	8
00A0-00A1	Interrupt Controller 2	8
00C0-00DF	DMA Controller 2	8
00F0-00FF	Co-processor error	
0170-0177, 0376	Secondary IDE Controller	
01F0-01F7	Primary IDE Controller	
0278-027F	Parallel Port 3	
02E8-02EF	Serial Port 4	
02F8-02FF	Serial Port 2	
0370-0377	Secondary Floppy Disk Controller	
0378-037F	Parallel Port 2	
03B0-03DF	Integrated Video Graphics Controller	
03C0-03DF	Integrated Video Graphics Controller	

I/O Address Ports	Function	Bits
03BC-03BF	Parallel Port 1	
03F0--03F5-03F7	Integrated Floppy Disk Controller	
03F8-03FF	Serial Port 1	
03E8-03EF	Serial Port 3	
0CF8-0CFF	Used for PCI Configuration[1]	
0496-0497	HP Reserved	
0678-067A	Parallel Port if ECP Mode is Selected	
0778-077A	Parallel Port if ECP Mode is Selected	

[1] These addresses are dedicated to configuration registers for PCI devices.

Addressing System Board Components (BIOS version: GJ.07.xx)

This section provides further details of how the BIOS uses the system board components mentioned in the I/O port list.

DMA Channel Controllers (BIOS version: GJ.07.xx)

Only “I/O-to-memory” and “memory-to-I/O” transfers are allowed. “I/O-to-I/O” and “memory-to-memory” transfers are disallowed by the hardware configuration.

The system controller supports seven DMA channels, each with a page register used to extend the addressing range of the channel to 16 MB.

The following table summarizes how the DMA channels are allocated.

First DMA controller (used for 8-bit transfers)	
Channel	**Function**
0	Available
1	Available or ECP mode for parallel port
2	Floppy disk I/O
3	Available or ECP mode for parallel port
Second DMA controller (used for 16-bit transfers)	
Channel	**Function**
4	Cascade from first DMA controller
5-6	Available
6-7	Available

Interrupt Controllers

(BIOS version: GJ.07.xx)

The system has two 8259A compatible interrupt controllers. They are arranged as a master interrupt controller and a slave that is cascaded through the master.

The following table shows how the master and slave controllers are connected. As the HP Vectra 500 Series incorporates the Plug and Play mode, some of the IRQ settings indicated in the following table could be different. This table should be used as a guideline only. The Interrupt Requests (IRQ) are numbered sequentially, starting with the master controller, and followed by the slave.

IRQ (Interrupt Vector)		Interrupt Request Description
IRQ0(08h)		System timer
IRQ1(09h)		Keyboard controller
IRQ2(0Ah)	Slave IRQ	Cascade connection from INTC2 (Interrupt Controller 2)
	IRQ8(70h)	Real time clock
	IRQ9(71h)	Available for PCI expansion cards, if not used by ISA boards
	IRQ10(72h)	Available for PCI expansion cards, if not used by ISA boards
	IRQ11(73h)	Available for PCI expansion cards, if not used by ISA boards

	IRQ12(74h)	Mouse
	IRQ13(75h)	Pentium processor
	IRQ14(76h)	Integrated primary IDE hard disk controller
	IRQ15(77h)	Free, if not used by secondary channel of IDE controller[1] (CD-ROM)
IRQ3(0Bh)		Free, if not used used for serial port[2]
IRQ4(0Ch)		Free, if not used used for communications card or serial port[2]
IRQ5(0Dh)[3]		Free, if not used used for expansion card or parallel port[4]
IRQ6(0Eh)		Floppy disk drive controller
IRQ7(0Fh)		Free, if not used used for parallel port[3]

1. IRQ15 can be made available by disabling the secondary channel of the IDE controller in the SETUP program.
2. IRQ3 and IRQ4 can be made available by disabling the serial ports in the SETUP program.
3. If there is a need to use another IRQ for the sound card, the following Interrupt Vectors can be used: IRQ2, IRQ7 and IRQ10.
4. IRQ5 and IRQ7 can be made available by disabling the parallel ports in the SETUP program.

PCI Interrupt Request Lines

(BIOS version: GJ.07.xx)

PCI devices generate interrupt requests using up to four PCI interrupt request lines (INTA#, INTB#, INTC#, and INTD#).

When a PCI device makes an interrupt request, the request is re-directed to the system interrupt controller. The interrupt request will be re-directed to one of the IRQ lines made available for PCI devices.

All PCI devices with interrupt transfer support will use and share INTA#. A multiple-function PCI device may use several INT lines. These devices will require more than one system interrupt request line.

Power-On Self-Test (BIOS version: GJ.07.xx)

This section describes the Power-On Self-Test (POST) routines, which are contained in the PC's ROM BIOS, the error messages which can result, and the suggestions for corrective action.

Each time the system is powered on, or a reset is performed, the POST is executed. The POST process verifies the basic functionality of the system components and initializes certain system parameters. The POST performs the tests in the order described in the table on the next page.

The POST displays a graphic screen with the HP Vectra logo. If the POST detects an error, the error message is displayed. To see the tests performed during the POST, press Esc when the initial HP "Vectra" logo appears, and the display will switch to text mode. In this mode, a summary configuration screen will be displayed at the end of the POST. Pressing the PAUSE/ BREAK key at any time will allow you to inspect the screen contents. Press any key to resume.

Devices such as the slave disks are validated in the *Setup* program. You are prompted if a device is found to have gone missing since the previous boot.

During the POST, the BIOS and other ROM data are copied into high-speed shadow RAM. The shadow RAM is addressed at the same physical location as the original ROM in a manner which is completely transparent to applications. It therefore appears to behave as very fast ROM. This technique provides faster access to the system BIOS firmware.

If the POST is initiated by a soft reset Ctrl Alt and Delete, the RAM tests are not executed and shadow RAM is not cleared. In all other respects, the POST executes in the same way following power-on or a soft reset.

NOTE

The POST does not detect when a *slave hard disk drive* ("HDD 1" or "HDD 3" in the setup) has been installed or changed.

Shadow Ram (BIOS version: GJ.07.xx)

On HP personal computers, access to certain ROM data is enhanced by using shadow RAM. During the POST, the BIOS and other ROM data are copied into high-speed shadow RAM. The shadow RAM is addressed at the same physical location as the original ROM in a manner which is completely transparent to applications. This technique provides faster access to the system BIOS firmware.

POST Test	Description
System BIOS Tests	
LED Test	Tests the LEDs on the control panel.
Processor Test	Tests the processor's registers. Test failure causes the boot process to abort.
System (BIOS) ROM Test	Calculates an 8-bit checksum. Test failure causes the boot process to abort.
RAM Refresh Timer Test	Tests the RAM refresh timer circuitry. Test failure causes the boot process to abort.
Interrupt RAM Test	Checks the first 64 KB of system RAM used to store data corresponding to various system interrupt vector addresses. Test failures cause the boot process to abort.
Shadow the System ROM BIOS	Tests the system ROM BIOS and shadows it. Failure to shadow the ROM BIOS will cause an error code to display. The boot process will continue, but the system will execute from ROM. This test is not performed after a soft reset (using Ctrl Alt and Delete).
Load CMOS Memory	Checks the serial EEPROM and returns an error code if it has been corrupted. Copies the contents of the EEPROM into CMOS RAM.
CMOS RAM Test	Checks the CMOS RAM for start-up power loss, verifies the CMOS RAM checksum(s). Test failure causes error codes to display.
Internal Cache Memory Test	Tests the processor's internal level-one cache RAM. Test failure causes an error code to display and the boot process to abort.
Video Tests	
Initialize the Video	Initializes the video subsystem, tests the video shadow RAM, and, if required, shadows the video BIOS. A failure causes an error code to display, but the boot process continues.

System Board Tests	
Test External Cache	Tests the level-two cache. A failure causes an error code to display and disables the external cache.
Shadow SCSI ROM	Tests for the presence of HP SCSI ROMs. If SCSI ROMs are detected, their contents are copied into the shadow RAM area. A failure will cause an error code to display.
8042 Self-Test	Downloads the 8042 and invokes the 8042 internal self-test. A failure causes an error code to display.
Timer 0/Timer 2 Test	Tests Timer 0 and Timer 2. Test failure causes an error code to display.
DMA Subsystem Test	Checks the DMA controller registers. Test failure causes an error code to display.
Interrupt Controller Test	Tests the Interrupt masks, the master controller interrupt path (by forcing an IRQ0), and the industry-standard slave controller (by forcing an IRQ8). Test failure causes an error code to display.
Real-Time Clock Test	Checks the real-time clock registers and performs a test that ensures that the clock is running. Test failure causes an error code to display.
Memory Tests	
RAM Address Line Independence Test	Verifies the address independence of real-mode RAM (no address lines stuck together). Test failure causes an error code to display.
Size Extended Memory	Sizes and clears the protected mode (extended) memory and writes the value into CMOS bytes 30h and 31h. If the system fails to switch to protected mode, an error code is displayed.
Real-Mode Memory Test (First 640KB)	Read/write test on real-mode RAM. (This test is *not* done during a reset using Ctrl Alt and Delete). The test checks each block of system RAM to determine how much is present. Test failure of a 64 KB block of memory causes an error code to display, and the test is aborted.
Shadow RAM Test	Tests shadow RAM in 64-KB segments (except for segments beginning at A000h, B000h, and F000h). If they are *not* being used, segments C000h, D000h and E000h are tested. Test failure causes an error code to display.
Protected Mode RAM Test (Extended RAM)	Tests protected RAM in 64-KB segments above 1 MB. (This test is *not* done during a reset using Ctrl Alt and Delete). Test failure causes an error code to display.
Keyboard / Mouse Tests	
Keyboard Test	Invokes a built-in keyboard self-test of the keyboard's microprocessor and tests for the presence of a keyboard and for stuck keyboard keys. Test failure causes an error code to display.
Mouse Test	If a mouse is present, invokes a built-in mouse self-test of the mouse's microprocessor and for stuck mouse buttons. Test failure causes an error code to display.

Tests of Flexible Disk Drive A	
Flexible Disk Controller Subsystem Test	Tests for proper operation of the flexible disk controller. Test failure causes an error code to display.
Coprocessor Tests	
Internal Numeric Coprocessor Test	Checks for proper operation of the numeric coprocessor part of the processor. Test failure causes an error code to display.
Parallel Port Tests	
Parallel Port Test	Tests the integrated parallel port registers, as well as any other parallel ports. Test failure causes an error code to display.
Serial Port Tests	
Serial Port Test	Tests the integrated serial port registers, as well as any other serial ports. Test failure causes an error code to display.
Hard Disk Drive Tests	
Hard Disk Controller Subsystem Test	Tests for proper operation of the hard disk controller. Test failure causes an error code to display. The test does not detect hard disk replacement or changes in the size of the hard disk.
System Configuration Tests	
System Generation	Initiation of the system generation (SYSGEN) process, which compares the configuration information stored in the CMOS memory with the actual system. If a discrepancy is found, an error code will be displayed.
Plug and Play Configuration	Configures any Plug and Play device detected (either PCI or ISA): ❒ All PCI devices and any ISA device necessary for loading the operating system will be configured for use. ❒ Any ISA device that is not required for loading the operating system will be initialized (prepared for loading of a device driver), but not fully configured for use.

Error Messages (BIOS version: GJ.07.xx)

When the PC is switched on or reset, a power-on hardware test is performed. If an error occurs, an error message is displayed.

NOTE:

HP's new-style BIOS does not display POST error codes (such as 910B). These were displayed in the BIOS of previous HP Vectra PCs.

Message	Corrective Action and/or Explanation
Operating system not found	Check whether the disk, HDD, FDD or CD-ROM disk drive is connected. If it is connected, check that it is detected by POST. Check that your boot device is enabled on the *Setup* Security menu. If the problem persists, check that the boot device contains the operating system.
Missing operating system	If you have configured HDD user parameters, check that they are correct. Otherwise, use HDD -type "Auto" parameters.
Failure fixed disk (preceded by a 30" time-out)	Check that HDD is connected. Check that HDD is detected by POST. Check that boot on hard disk drive is enabled in *Setup*.
Diskette Drive A (or B) error	Check whether the diskette drive is connected. Check *Setup* for the configuration.
System battery is dead	You may get this message if the PC is disconnected for a few days. When you power-on the PC, run *Setup* to update the configuration information. The message should no longer be displayed. Should the problem persist, replace the battery.
Keyboard error	Check that the keyboard is connected.
Resource Allocation Conflict -PCI device 0079 on system board	Clear CMOS.
Video Plug and Play interrupted or failed Re-enable in Setup and try again	You may have powered your PC Off/On too quickly and the PC turned off Video plug and play as a protection.
System CMOS checksum bad - run Setup	CMOS contents have changed between 2 power-on sessions. Run *Setup* for configuration.
I/O device IRQ conflict	Serial ports A and B may have been assigned the same IRQ. Assign a different IRQ to each serial port and save the configuration.
No message, system "hangs" after POST	Check that cache memory and main memory are correctly set in their sockets.

Message	Corrective Action and/or Explanation
Other	An error message may be displayed and the PC may "hang" for 20 seconds and then beep. The POST is probably checking for a mass storage device which it cannot find and the PC is in Timeout Mode. After Timeout, run *Setup* to check the configuration.

Beep Codes (BIOS version: GJ.07.xx)

If a terminal error occurs during POST, the system issues a beep code before attempting to display the error. Beep codes are useful for identifying the error when the system is unable to display the error message.

Beep Pattern	Numeric Code	Description
	B4	This does not indicate an error. There is one short beep before system startup.
	98	Video configuration failure or Option ROMs checksum failure
	16H	BIOS ROM checksum failure
	20H	DRAM refresh test failure
	22H	8742 Keyboard controller test failure
	2C	RAM failure
	2E	RAM failure on data bits in low byte of memory bus
	30	RAM failure on data bits in high byte of memory bus
	46	ROM copyright notice check failure
	58	Unexpected interrupts test failure

5

Video Controllers

This chapter gives details of the three types of video subsystems used by the HP Vectra 500 Series computers. These video subsystems are: the SiS 6250 and S3 Trio 64 PnP video controllers, both of which are integrated on the system board, and the Matrox MGA Millennium video card.

SiS 6205 Video Controller

The SiS 6205 video controller supports UMA architecture, and therefore no dedicated video memory is loaded on the system board. The shared frame buffer is located in the system DRAM and the memory access bus and memory data bus.

The SiS 6205 video controller offers full compatibility with VGA. In addition, the features are enhanced beyond the Super VGA by hardware which accelerates graphical user interface operation in Windows 95.

The SiS 6205 video controller is installed on the HP Vectra 500 Series PC models with part number D4051-63001. For a complete list of the computers associated with this part number, refer to “D4051-63001 Models” on page 15.

SiS 6205 Video Controller Summary

The video subsystem uses the PCI bus for data transfers between the processor and the video subsystem, and has the following features:

- 64-bit video memory access with 1 or 2 MB of video memory.
- Support for up to 2 MB DRAM at 60 ns.
- Graphics resolutions of up to 1280 x 1023 with 2 MB.
- Integrated 24-bit RAMDAC.
- Green PC power-saving features.
- Standard and Enhanced Video Graphics Array (VGA) modes.
- DDC 2B compliant.

	HP Vectra 500 Series with the SiS 6205 Chip	Upgradeable to:
Video Controllers	SIS 6205 Video Controller	
Hardware Acceleration of major graphics operations to speed up applications using graphical user interfaces (GUIs)	Yes	
DRAM support	1 MB of 60 ns resident in main memory.	2 MB by using the HP Setup program, or Using the HP Dynamic Video Feature, on page 118.
Graphics Resolutions	Up to 1280 x 1023	
Pixel Clock (Max.)	135 MHz	

Upgrading Video Memory (UMA)

The default setting for the video memory is 1 MB. The video memory is resident in the main memory, so if there is 12 MB of main memory, 1 MB of this is allocated to the video memory.

To increase the amount of video memory from 1 MB up to the maximum of 2 MB, there is no need to physically install any video memory modules. If we use the above example of 12 MB of main memory, this means that setting the video memory to 2 MB would leave 10 MB for the main memory.

This is useful when there is a need to upgrade the video memory for applications that will need more than 1 MB. This can then be switched back to the original setting when finished.

The video memory can be upgraded either by using the HP Setup program or from within Windows 95.

Using the HP Dynamic Video Feature

To increase the amount of video memory using the HP Dynamic video feature, follow these steps:

- Click the Start button.
- Select Settings, then Control Panel.
- Double-click the Display icon.
- Click the HP Dynamic Video tab.
- Drag the Video Memory slider from 1 MB to 2 MB. (The System memory value is automatically adjusted).
- Click the OK button and then restart your computer for the video memory configuration to take effect.

Typical Windows 95 Video Resolutions (SiS 6205 Chip)

The following are typical Windows 95 video resolutions that are supported by the SiS 6205 video controller.

Resolution	Number of colors	Refresh Rate (Hz)	Memory
640 x 480	16	60	1 MB
640 x 480	256, 64K, 16M	60, 72, 75, 85	
800 x 600	256, 64K	56, 60, 72, 75, 85	
1024 x 768	256	i43[1] 60, 70, 75, 85	

Resolution	Number of colors	Refresh Rate (Hz)	Memory
640 x 480	16	60	2 MB
640 x 480	256, 64K, 16M	60, 72, 75, 85	
800 x 600	256, 64K, 16M	56, 60, 72, 75, 85	
1024 x 768	256, 64K	i43[1], 60, 70, 75, 85	
1280 x 1023	256	i43[1], 60, 75	

1. Interlaced.

VESA Feature Connector (SiS 6205 Chip)

The Video Electronics Standards Association (VESA) defines a standard video connector, variously known as the VESA feature connector, auxiliary connector, or pass-through connector. The integrated video controller supports an output-only VESA feature connector. This connector is integrated directly on the system board and is connected directly to the pixel data bus and the synchronization signals.

The Integrated Ultra VGA Video Controller

The Integrated Ultra VGA video controller is installed on the HP Vectra 500 Series PC models with part number D3657-63001. For a complete list of the computers associated with this part number, refer to “D4051-63001 Models” on page 15

S3 Trio 64 Video Controller Summary

The video subsystem uses the PCI bus for data transfers between the processor and the video subsystem, and has the following features:

- 100% compatible with IBM VGA display standard.
- 32-bit video memory access with 1 MB DRAM. This increases to 64-bit access when an additional 1 MB DRAM is installed.
- Hardware acceleration of graphical user interface (GUI) operations.
- Support for up to 2 MB DRAM at 60 ns.
- Graphics resolutions of up to 1280 x 1024 with 2MB.
- Integrated 24-bit RAMDAC.
- Green PC power saving features.
- Standard and Enhanced Video Graphics Array (VGA) modes.
- DDC 1 compliant.

	HP Vectra 500 Series with the S3 Trio 64 PnP Chip	Upgradeable to:
Video Controller	Integrated 64-bit Ultra VGA on PCI bus (S3 Trio 64 PnP).	
Hardware Acceleration of major graphics operations to speed up applications using graphical user interfaces (GUIs)	yes.	
DRAM support	1-2 MB of 60 ns . 1 MB preinstalled.	2 MB (pair of 512KB modules)
Graphics Resolutions Up to	1280 x 1024.	
Pixel Clock (Max.)	135 MHz.	

S3 Trio 64 Video Memory

The S3 Trio 64 PnP integrated video subsystem has 1 MB of video DRAM preinstalled on the system board, and provides two sockets for the installation of a pair of 512KB video DRAM chips, to upgrade to video memory to 2 MB. The installed video memory capacity is detected automatically by the BIOS.

Normally, the controller gives 32-bit video memory access, with 1 MB of video RAM fitted. This is increased to 64-bit access when the additional 1 MB upgrade is installed.

When the upgrade modules are installed, care must be exercised to align the tapered end of the module with the tapered end of the socket on the system board. A special extraction tool (5041-2553) is needed when removing the modules.

S3 Trio 64 Video Modes

The video subsystem is responsible for generating video data (which is placed in video memory) to be sent to the display.

The following table details the Standard and Enhanced Video Graphics Array (VGA) modes which are currently implemented in the video BIOS. These modes are supported by standard BIOS functions; that is, the video BIOS (which is mapped contiguously in the address range C0000h to C7FFFh) contains all the routines required to configure and access the video subsystem.

Standard VGA Modes (S3 Trio 64)

Mode No.	Standard	Interface Type	Resolution	No. of Colors	Vertical Refresh (Hz)	Horizontal Refresh (kHz)	Dot Clock (MHz)
00h	VGA	text	40 x 25 chars	b/w	70	31.5	25.175
00h	VGA	text	40 x 25 chars	b/w	70	31.5	25.175
00h+	VGA	text	40 x 25 chars	b/w	70	31.5	28.322
01h	VGA	text	40 x 25 chars	16	70	31.5	25.175
01h	VGA	text	40 x 25 chars	16	70	31.5	25.175
01h+	VGA	text	40 x 25 chars	16	70	31.5	28.322
02h	VGA	text	80 x 25 chars	b/w	70	31.5	25.175
02h	VGA	text	80 x 25 chars	b/w	70	31.5	25.175
02h+	VGA	text	80 x 25 chars	b/w	70	31.5	28.322
03h	VGA	text	80 x 25 chars	16	70	31.5	25.175

Mode No.	Standard	Interface Type	Resolution	No. of Colors	Vertical Refresh (Hz)	Horizontal Refresh (kHz)	Dot Clock (MHz)
03h	VGA	text	80 x 25 chars	16	70	31.5	25.175
03h+	VGA	text	80 x 25 chars	16	70	31.5	28.322
04h	VGA	graph	320 x 200	4	70	31.5	25.175
05h	VGA	graph	320 x 200	4	70	31.5	25.175
06h	VGA	graph	640 x 200	2	70	31.5	25.175
07h	VGA	text	80 x 25 chars	Mono	70	31.5	28.322
07h+	VGA	text	80 x 25 chars	Mono	70	31.5	28.322
0Dh	VGA	graph	320 x 200	16	70	31.5	25.175
0Eh	VGA	graph	640 x 200	16	70	31.5	25.175
0Fh	VGA	graph	640 x 350	Mono	70	31.5	25.175
10h	VGA	graph	640 x 350	16	70	31.5	25.175
11h	VGA	graph	640 x 480	2	60	31.5	25.175
12h	VGA	graph	640 x 480	16	60	31.5	25.175
13h	VGA	graph	320 x 200	256	70	31.5	25.175

Extended Video Modes with 1 MB DRAM (S3 Trio 64)

VESA Mode No.	Extended Mode No.	Interface Type	Resolution	No. of Colors	Vertical Refresh (Hz)	Horizontal Refresh (kHz)	Dot Clock (MHz)
10Ah	54h	text	132 x 43 chars	16	70	31.5	40.000
109h	55h	text	132 x 25 chars	16	70	31.5	40.000
100h	68h	graph	640 x 400	256	70	31.5	25.175
101h	69h	graph	640 x 480	256	60	31.5	25.175
101h	69h	graph	640 x 480	256	72	37.9	31.500
101h	69h	graph	640 x 480	256	75	37.5	31.500
102h	6Ah	graph	800 x 600	16	56	35.1	36.000
102h	6Ah	graph	800 x 600	16	60	37.9	40.000
102h	6Ah	graph	800 x 600	16	72	48.1	50.000
102h	6Ah	graph	800 x 600	16	75	47.5	49.500
103h	6Bh	graph	800 x 600	256	56	35.1	36.000
103h	6Bh	graph	800 x 600	256	60	37.9	40.000
103h	6Bh	graph	800 x 600	256	72	48.1	50.000
103h	6Bh	graph	800 x 600	256	75	46.8	49.500
104h	6Ch	graph	1024 x 768	16	43 (i)	35.5	44.900
104h	6Ch	graph	1024 x 768	16	60	48.4	65.000
104h	6Ch	graph	1024 x 768	16	70	56.5	75.000

VESA Mode No.	Extended Mode No.	Interface Type	Resolution	No. of Colors	Vertical Refresh (Hz)	Horizontal Refresh (kHz)	Dot Clock (MHz)
104h	6Ch	graph	1024 x 768	16	75	60.2	80.000
105h	6Dh	graph	1024 x 768	256	43 (i)	35.5	44.900
105h	6Dh	graph	1024 x 768	256	60	48.4	65.000
105h	6Dh	graph	1024 x 768	256	70	56.5	75.000
105h	6Dh	graph	1024 x 768	256	75	60.2	80.000
106h	6Eh	graph	1280 x 1024	16	45 (i)	47.7	75.000
107h	6Fh	graph	1280 x 1024	256	45 (i)	47.7	37.500 x 2
107h	6Fh	graph	1280 x 1024	256	60	63.7	55.000 x 2
107h	6Fh	graph	1280 x 1024	256	72	77.7	65.000 x 2
107h	6Fh	graph	1280 x 1024	256	75	79.5	67.500 x 2
110h	70h	graph	640 x 480	32 K	60	31.5	25.175
110h	70h	graph	640 x 480	32 K	72	37.5	31.500
110h	70h	graph	640 x 480	32 K	75	37.5	31.500
111h	71h	graph	640 x 480	64	60	31.5	25.175
111h	71h	graph	640 x 480	64	72	37.5	31.500
111h	71h	graph	640 x 480	64	75	37.5	31.500
112h	72h	graph	640 x 480	16 M	60	31.5	25.175
112h	72h	graph	640 x 480	16 M	72	37.9	31.500
112h	72h	graph	640 x 480	16 M	75	37.5	31.500
113h	73h	graph	800 x 600	32 K	60	37.9	40.000
113h	73h	graph	800 x 600	32 K	72	48.1	50.000
113h	73h	graph	800 x 600	32 K	75	46.8	49.500
114h	74h	graph	800 x 600	64	60	37.9	40.000
114h	74h	graph	800 x 600	64	72	48.1	50.000
114h	74h	graph	800 x 600	64	75	46.8	49.500
115	75h	graph	800 x 600	16 M	60	37.9	40.000
115	75h	graph	800 x 600	16 M	72	48.1	50.000
115	75h	graph	800 x 600	16 M	75	46.8	49.500
116	76h	graph	1024 x 768	32 K	43 (i)	35	44.900
116	76h	graph	1024 x 768	32 K	60	48.9	65.000
116	76h	graph	1024 x 768	32 K	70	56.5	75.000
116	76h	graph	1024 x 768	32 K	75	60.4	80.000
117	77h	graph	1024 x 768	64	43 (i)	35	44.900
117	77h	graph	1024 x 768	64	60	48.9	65.000
117	77h	graph	1024 x 768	64	70	56.5	75.000
117	77h	graph	1024 x 768	64	75	60.4	80.000
118	78h	graph	1024 x 768	16 M	43 (i)	35.2	44.900
119	79h	graph	1280 x 1024	32 K	45 (i)	48.7	75.000
11A	7A	graph	1280 x 1024	64	45 (i)	48.7	75.000

VESA Mode No.	Extended Mode No.	Interface Type	Resolution	No. of Colors	Vertical Refresh (Hz)	Horizontal Refresh (kHz)	Dot Clock (MHz)
120	7c	graph	1600 x 1200	256	48.5 (i)	62	65.000 x 2
201	49	graph	640 x 480	256	60	31.5	25.175
201	49	graph	640 x 480	256	72	37.9	31.500
201	49	graph	640 x 480	256	75	37.5	31.500
202	4A	graph	800 x 600	16	56	35.1	36.000
202	4A	graph	800 x 600	16	60	37.9	40.000
202	4A	graph	800 x 600	16	72	48.1	50.000
202	4A	graph	800 x 600	16	75	46.9	49.500
203	4B	graph	800 x 600	256	56	35.1	36.000
203	4B	graph	800 x 600	256	60	37.9	40.000
203	4B	graph	800 x 600	256	72	48.1	50.000
203	4B	graph	800 x 600	256	75	46.8	49.500
204	4C	graph	1024 x 768	16	43 (i)	35.5	44.900
204	4C	graph	1024 x 768	16	60	48.4	65.000
204	4C	graph	1024 x 768	16	70	56.5	75.000
204	4C	graph	1024 x 768	16	75	60.3	80.000
205	4D	graph	1024 x 768	256	60	48.4	44.900
205	4D	graph	1024 x 768	256	70	56.5	65.000
205	4D	graph	1024 x 768	256	75	60.2	75.000
205	4D	graph	1024 x 768	256	75	60.2	80.000
207h	4Eh	graph	1152 x 864	256	60	55.3	80.000
208h	4Fh	graph	1280 x 1024	16	43 (i)	47.7	37.500 x 2
208h	4Fh	graph	1280 x 1024	16	60	63.7	55.000 x 2
208h	4Fh	graph	1280 x 1024	16	72	77.7	65.000 x 2
208h	4Fh	graph	1280 x 1024	16	75	79.8	65.000 x 2
i = interlaced							

Extended Video Modes with 2 MB DRAM (S3 Trio 64)

VESA Mode No.	Extended Mode No.	Interface Type	Resolution	No. of Colors	Vertical Refresh (Hz)	Horizontal Refresh (kHz)	Dot Clock (MHz)
107h	6Fh	graph	1280 x 1024	256	45 (i)	47.7	37.500 x 2
107h	6Fh	graph	1280 x 1024	256	60	63.7	55.000 x 2
107h	6Fh	graph	1280 x 1024	256	72	77.7	65.000 x 2
107h	6Fh	graph	1280 x 1024	256	75	79.5	67.500 x 2
115h	75h	graph	800 x 600	16. M	60	37.9	40.000
115h	75h	graph	800 x 600	16. M	72	41.8	50.000
115h	75h	graph	800 x 600	16. M	75	46.8	49.500
116h	76h	graph	1024 x 768	32 K	43i	35	44.900
116h	76h	graph	1024 x 768	32 K	60	48.9	65.000
116h	76h	graph	1024 x 768	32 K	70	56.5	75.000
116h	76h	graph	1024 x 768	32 K	75	60.2	80.000
116h	76h	graph	1024 x 768	32 K	85	68.7	95.000
117h	77h	graph	1024 x 768	64	43i	35	44.900
117h	77h	graph	1024 x 768	64	60	48.9	65.000
117h	77h	graph	1024 x 768	64	70	56.5	75.000

Typical Windows 95 Video Resolutions (S3 Trio 64)

Resolution	Number of colors	Refresh Rate (Hz)	Memory
640 x 480	16	60	1 MB
640 x 480	256, 64K	60, 72, 75	
800 x 600	256, 64K	56, 60, 72, 75	
1024 x 768	256	i43[1] 60, 70, 75	

Resolution	Number of colors	Refresh Rate (Hz)	Memory
640 x 480	16	60	2 MB
640 x 480	256, 64K, 16M	60, 72, 75	
800 x 600	256, 64K, 16M	56, 60, 72, 75	
1024 x 768	256, 64K	i43[1], 60, 70, 75	
1280 x 1024	256	i45[1], 60, 72, 75	

1. Interlaced.

VESA Connector

The Video Electronics Standards Association (VESA) defines a standard video connector, variously known as the VESA *feature* connector, *auxiliary* connector, or *pass-through* connector. The integrated video controller supports an output-only VESA *feature* connector. This connector is integrated directly on the system board, and is connected directly to the pixel data bus and the synchronization signals.

To use the VESA feature connector in DOS, or Windows 95, the FCON.EXE utility must be executed. This utility configures the system.

WARNING

Use of the VESA feature connector will disable the 1 MB video memory upgrade, if this has been installed. Only the standard 1 MB of video memory will be used.

Matrox MGA Millennium Video Controller Card

The Matrox MGA Millennium PCI video controller is installed in a PCI expansion slot. Its on-card MGA-2064W processor communicates with the Pentium Pro processor along the PCI bus.

The Matrox MGA Millennium video controller is installed on the HP Vectra 500 Series PC models with system board part number D3661-63001. For a complete list of the computers associated with this part number, refer to “D3661-63001 Model” on page 17.

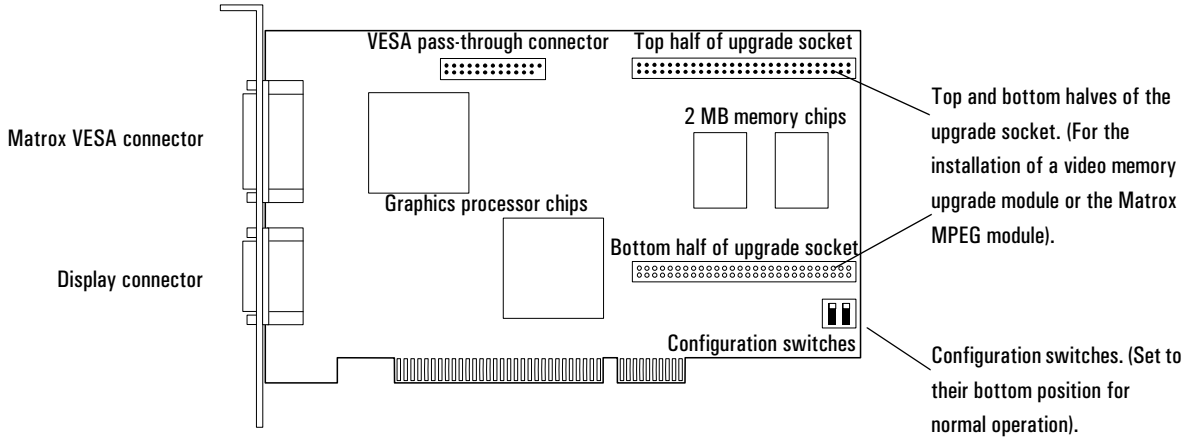
The controller can be characterized as follows:

- 100% hardware- and BIOS-compatible with IBM® VGA display standard.
- 64-bit video memory access.
- Hardware acceleration of graphical user interface (GUI) operations.
- Support for up to 8 MB Window RAM (WRAM) at 60 ns.
- Integrated 24-bit, 175 MHz RAMDAC.
- Pixel clock maximum frequency of 135 MHz.
- Green PC power-saving features.
- Standard and Enhanced Video Graphics Array (VGA) modes.
- Acceleration for 3D, playback, MPEG (when an optional upgrade module from Matrox is fitted), continuous interpolation on X, replication on Y, acceleration at true color.
- DDC 2B compliant.

MGA Connectors

The Video Electronics Standards Association (VESA) defines a standard video connector, variously known as the VESA *feature* connector, *auxiliary* connector, or *pass-through* connector. The video controller supports an output-only VESA *feature* connector in VGA mode. This connector is integrated on the PCI card, and is connected directly to the pixel data bus and the synchronization signals.

There are two connectors on the back panel: the normal DB15 VGA connector for connecting to HP displays, and a Matrox VESA connector.



If you install a VESA-standard video expansion card that uses the MGA video adapter, connect the expansion card's cable to the VESA pass-through connector on the card.

MGA Video Memory

The video memory (also known as window RAM, or WRAM) is a local block of RAM for holding two major data structures: the double buffer (to hold one frame steady on the screen whilst the next one is being processed), and the Z-buffer (for storing depth information for each pixel). It is dual-ported, so that it can be input and output simultaneously.

The Matrox MGA Millennium video card is supplied with 2 MB of video memory. This can be upgraded to 4 MB with a D3557A upgrade module, or to 8 MB with an MGA-MIL/MOD6 upgrade module (ordered from Matrox). The upgrade socket can alternatively be used for the installation of the Matrox MGA Media XL upgrade module (also ordered from Matrox) to support MPEG. The switch settings do not have to be changed.

Available MGA Video Resolutions

The number of colors supported is limited by the video card and the video memory. The resolution/refresh-rate combination is limited by a combination of the display, the graphics card, and the video memory.

If you attempt to set the resolution or number of colors higher than is supported by the installed video memory, the screen refresh rate is lowered automatically, and image flicker becomes more noticeable. If the resolution/refresh-rate combination is set higher than the display can support, you risk damaging the display.

Resolution	Number of colors	Video Adapter Maximum Refresh Rate (Hz)	Memory
640 x 480	256, 64K, 16M	120	2 MB
800 x 600	256, 64K, 16M		
1024 x 768	256, 64K		
1280 x 1024	256	90	
1600 x 1200[1]	256	72	
640 x 480	256, 64K, 16M	120	4 MB
800 x 600	256, 64K, 16M		
1024 x 768	256, 64K, 16M		
1280 x 1024	256, 64K, 16M (24 bpp)	90	
1600 x 1200[1]	256, 64K	72	
640 x 480	256, 64K, 16M	120	8 MB
800 x 600	256, 64K, 16M		
1024 x 768	256, 64K, 16M		
1280 x 1024	256, 64K, 16M	90	
1600 x 1200[1]	256, 64K, 16M	72	

1. The upper limit of refresh rate for HP monitors is 60Hz at this resolution.

Drivers are provided on the CD-ROM that is supplied with the PC for Windows 95.

The following table summarizes the video resolutions which are supported.

Number of Colors	256	64 K Hi-Color	16.7 M True-Color	16.7 M True-Color
Bits per Pixel	8	16	24	32
640 × 480	2 MB, 120 Hz			
800 × 600	2 MB, 120 Hz			
1024 × 768	2 MB, 120 Hz		4 MB, 120Hz	
1152 × 882[1]	2 MB, 100 Hz		4 MB, 100 Hz	
1280 × 1024	2 MB, 90 Hz	4 MB, 90 Hz		8 MB, 90 Hz
1600 × 1200[2]	2 MB, 72 Hz	4 MB, 72 Hz	8 MB, 72 Hz	Not supported

1. 1152 × 882 is not supported by HP displays
2. The upper limit of refresh rate for HP monitors is 60Hz at this resolution.

The maximum 2D resolutions for any given video memory capacity and color scale can be found from the following table:

Number of Colors	256	64 K Hi-Color	16.7 M True-Color	16.7 M True-Color
Bits per Pixel	8	16	24	32
2 MB	1600 × 1200	1024 × 768	800 × 600	800 × 600
4 MB	1600 × 1200	1600 × 1200	1280 × 1024	1152 × 882[1]
8 MB	1600 × 1200	1600 × 1200	1600 × 1200	Not supported

1. 1152 × 882 is not supported by HP displays

MGA Video BIOS

A feature of the Matrox MGA Millennium card is the capability to flash program the video BIOS. This is achieved as follows:

1 Set SW-1, on the Matrox card, to ON (BIOS unprotected).
2 Set the "Operating System" field in the *Setup* program to **`Others`**.
3 Run the **`updbios.bat`** command file (provided by HP), to execute the video BIOS flash program, **`progbios.exe`**, and the associated **`*.bin`** file.
4 Set SW-1, on the Matrox card, to OFF (BIOS protected).
5 Set the "Operating System" field in the *Setup* program back to an appropriate setting.

Video cards without ROM (such as old CGA and monochrome) are not supported by the BIOS. Memory holes above 1 MB are not supported. DDC display detection is not a BIOS feature, but is handled by the video drivers.

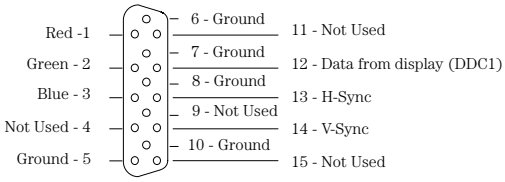
Further Information About MGA

For more information on the Matrox MGA Millennium video adapter card, contact Matrox Electronic Systems:

Matrox Electronic Systems Ltd.,
1055 St. Regis Blvd., Dorval, Quebec,
Canada H9P 2T4.
Telephone: (514) 685-2630; Fax: (514) 685-2853; BBS: (514) 685-6008

DB15 Connector Pinout

The layout of the pins for the DB15 VGA Connector are the same for the three video controllers mentioned earlier in this section.



6

Aztech AT3300 Audio Fax/Data Modem

Depending on the particular HP Vectra 500 Series PC model, there may be an Aztech AT3300 audio fax/data modem installed. This modem incorporates built-in advanced communication and audio telephony features, including a capability to perform simultaneous audio playback and recording, as well as hands-free communication.

Introduction

The Aztech AT3300 audio fax/data modem operates in Plug and Play mode, therefore the hardware settings should not conflict with those of any other devices on the system. The Windows 95 Device Manager can be used to check the type of modem and configuration installed on the PC.

The built-in full duplex Speakerphone communications option delivered with the HP Vectra 500 Series PC offers a complete business solution. It provides the latest state-of-the-art communications tools that give access to a world of communications possibilities. Not only is it possible to send and receive faxes, and receive voice messages, but also to access a huge store of information through Bulletin Board Systems (called BBSs). Files and computer software can be uploaded and downloaded to and from a BBS.

The Speakerphone communications option provides hands-free communication and multimedia functions, through the use of a headset and other audio devices. However, what will be appreciated most in the communications option is its telephone answering capabilities and the possibility for everyday modem-to-modem exchange of business faxes and files.

Service providers, including America Online, CompuServe, GEnie, and Prodigy, supply access to services such as electronic mail, airline reservations, banking and finance, and computer support forums.

The communications option is fully compliant with both U.S. and international communications standards. Compatibility with these standards ensures the possibility to communicate with other modems anywhere in the world.

Communications Options

As a data modem, the modem operates at line speeds of up to 28,800 bps. Error correction (V.42/MNP 2-4) and data compression (V.42 bis/MNP 5) maximize data transfer integrity and boost data throughput up to 115.2 kbps. The modem also operates in non-error-correcting mode.

Extended “AT” commands provide data, fax class 1 and class 2, and MNP 10 functions, while using minimal external ROM, RAM, and optional NVRAM.

The modem also operates over a dial-up telephone line, can autodial and autoanswer, and can operate in both synchronous and asynchronous modes.

As well as combining computer and telephone technologies, the communications option has the following features:

- 28,800-bps internal modem.
- Answering machine with multiple-voice mailboxes.
- Automatic baud rate recognition at all speeds.
- Autodial and autoanswer.
- Caller ID (available from the local telephone company) to screen incoming calls.
- Data modem throughput up to 115.2 kbps.

  V.34, V.FC, V.32 bis, V.32, V.22 bis, V.22A/B, V.23, and V.21; Bell 212A and 103.

  ITU V.42 bis and MNP 5 data compression.

  ITU V.42 and MNP 2-4 , MNP10, MNP 10EC error correction.
- Digitized speech compression or decompression or both.
- Enhanced ADPCM/PCM voice operation with concurrent DTMF detection.

- Fax modem send and receive rates of up to 14,400 bps.

  V.17/V.29/V.27ter and V21 channel 2, Group 3 Fax mode.
- Full duplex speakerphone.
- Enhanced AT, voice and class 1 & 2 fax commands.
- Line quality monitoring retrain.
- Recording of telephone conversation through the communication card.
- Support for external speakers.
- Tone or pulse dialing.

WARNING

In some countries, pulse dialing is not supported. This concerns the following countries: United Kingdom, Sweden, Netherlands and Norway.

- Up to 115,200-bps data transfers (V.34 with V.42 bis).
- Voice and data or fax operations in a single call, without having to hang up and redial.
- Voiceview - alternating voice and data.
- Voice monitoring function with auto fax/voice switch.

European Firmware and Telephone Line Configuration

The configuration of the Aztech AT3300 audio fax/data modem is specific to each country's telephone standards. The following table shows the different AT3300 European firmware configuration and telephone line interface.

Country	Firmware Country Code	Jumper Block Color	Pulse Dialing Supported
Denmark	003	Blue	No
Finland	004	Orange	Yes
France	005	Red	Yes
Germany	006	Black	Yes
Italy	008	Pink	Yes
Netherlands	010	Blue	No
Norway	011	White	No
Portugal	012	Blue	Yes
Spain	013	Yellow	Yes
Sweden	014	Purple	No
Switzerland	015	Gray	Yes
United Kingdom	016	Green	No

Configuring the firmware code

There are two ways in which the European firmware code on the Aztech AT3300 audio fax/data modem can be configured: by using the floppy disk utility, or manually with the HyperTerminal application.

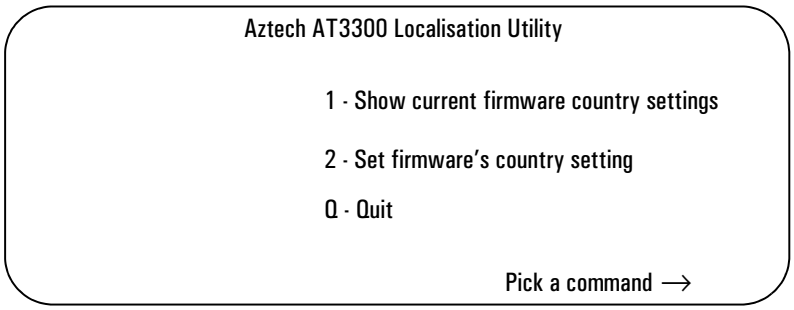
Aztech AT3300 Localisation Utility

The Aztech AT3300 Localisation Utility floppy disk automatically determines which firmware country code is configured on the Aztech AT3300 audio fax/data modem, and has the possibility to modify the configuration.

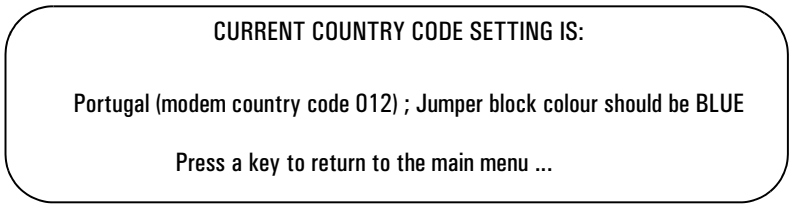
Using the Aztech AT3300 Localisation Utility

To use the Aztech AT3300 Localisation Utility, the system must be first shutdown, then rebooted on the Aztech 3300 Localisation Utility floppy disk.

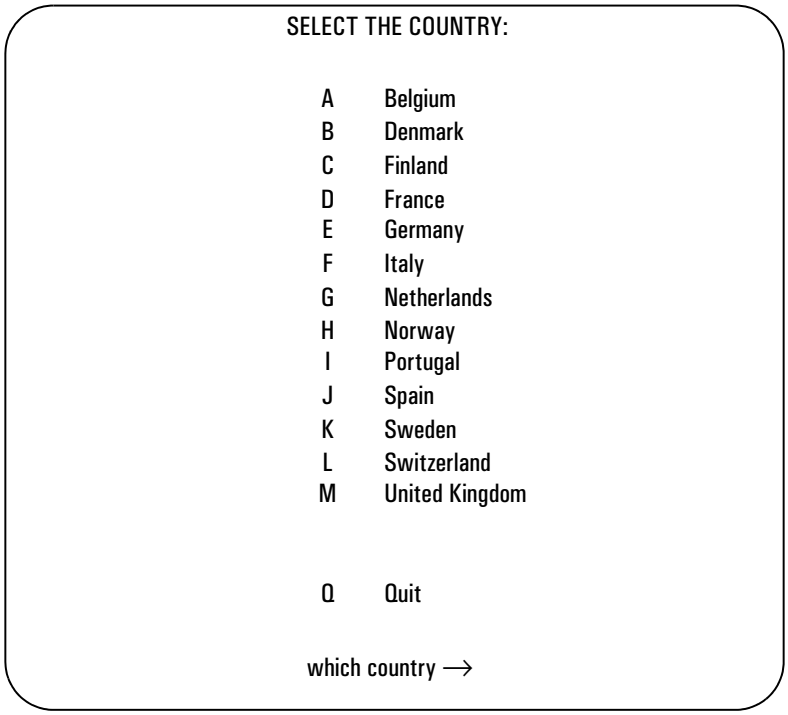
When the reboot has completed, the Localisation Utility main menu will appear:



Option 1 - shows the current firmware country code setting on the Aztech AT3300 audio fax/data modem. A screen similar to the following example will be displayed:



Option 2 - allows you to modify the country code setting to the desired configuration. Refer to the table on page 137 for the different country code settings.



1 Enter the letter that corresponds to the country to be configured.

The message,
"Please wait, reprogramming the modem"
will be displayed while the Audio Fax/Data Modem is reconfigured.

2 A window will then be displayed, indicating the modem firmware country code that has been set for the selected country, and the jumper block color setting.

3 To leave the Aztech AT3300 Localisation Utility:

Remove the Aztech AT3300 Localisation Utility floppy disk.

Ctrl Alt and Delete to reboot the PC.

4 After installing and localizing the Aztech AT3300 audio fax/data modem, you must then re-install the Mediatrends Quip software, since its license requires the card's identification. For details, see the Localization Instructions and Replacement Instructions notices which accompany the replacement card.

NOTE

Re-installing the Mediatrends Quip software requires the user password and a recorded blank message (this is the case, if no previous message has been recorded).

Using the HyperTerminal Application

By using the HyperTerminal application supplied with Windows 95, you can manually localize the firmware code for European configurations.

To use the HyperTerminal application:

- Click the Start button, point to Programs, then Accessories, then select HyperTerminal.
- Double click the Hypertrm.exe icon, and enter the name:

  AT3300 test
- Then click OK.

The Phone Number dialog box will then be displayed.

- Enter 11 in the Phone number box.
- Then click OK.

The Connect dialog box will then be displayed. Click cancel. Access to the HyperTerminal session will then follow, indicating its name (AT3300 test), as defined earlier.

Enter the following AT commands to verify or change the firmware country code:

AT Command	Comments	Modem Response	Comments
AT	tests that the PC and modem can communicate.	OK	modem confirmation
ATE1	enables character echo so that the modem commands appear on the screen.	OK	modem confirmation
ATI5 < cr >	shows the current country code.	xxx	current code configuration is displayed
		OK	modem confirmation.
AT*NCxxx < cr >	where xxx is the three digit firmware country code, as shown in the table on page 137.	OK	modem confirmation.
ATZ < cr >	resets the modem to the new configuration.	OK	modem confirmation.
ATI5 < cr >	verifies the current country code.	xxx	current code configuration is displayed
		OK	modem confirmation.

When you have finished, the HyperTerminal session can be saved and used again, or you can exit without saving the session.

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